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Next 25 Years—Part I:**

**FABRICS ON INTERCEPT COURSE WITH**

**VME's FUTURE**

**PLUS:**

**RoHS Adds New Wrinkle  
to Obsolescence**

**Tech Focus:  
Processor PMCs**



## Need reliability? -40° to +85°



**EPIC™ XE-900**  
**1.0 GHz CPU**

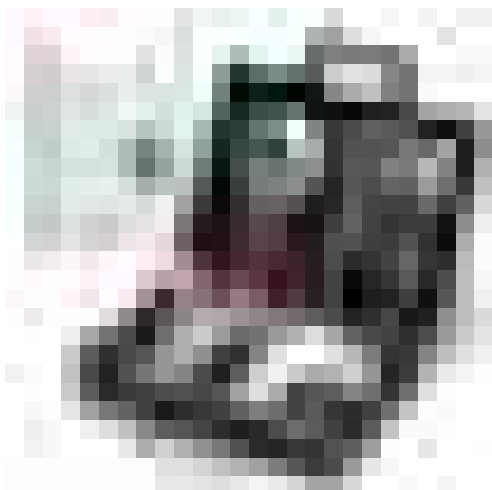
Features	XE-900	XE-800	XE-700
CPU	Via Eden	AMD Geode GXI	STPC
Clock speed	400 MHz; 733 MHz; 1.0 GHz	300 MHz	133 MHz
BIOS	General Software	Phoenix	Phoneix
DRAM support	to 256 MB	to 256 MB	32/64 MB
Compact/Flash	Type I or II	Type I or II	Type I or II
COM 1	RS-232	RS-232/422/485	RS-232
COM 2	RS-232	RS-232/422/485	RS-232/422/485
COM 3	RS-232	NA	RS-422/485
COM 4	RS-232	NA	RS-232
COM 5	RS-232/422/485	NA	NA
COM 6	RS-422/485/TTL	NA	NA
LPT 1	0	0	1
EIDE	2	2	1
USB	2	6	2
CRT	1600 x 1200	1280 x 1024	1280 x 1024
Flat panel	LVDS	yes	yes
Digital I/O	24-bit prog.	48-bit prog.	24-bit prog.
Ethernet	10/100 Base-T	Dual 10/100 Base-T	10/100 Base-T
Expansion	PC/104 & Plus	PC/104 & Plus	PC/104
Power	3.6A operating	1.6A max.	1.6A max
Temp. range	-40° to 70/85° C	-40° to 80° C	-40° to 80/85° C
Shock/vibration	40/5g	40/5g	40/5g

## Need Linux, QNX, Windows®? Try our OS EMBEDDER™ KITS

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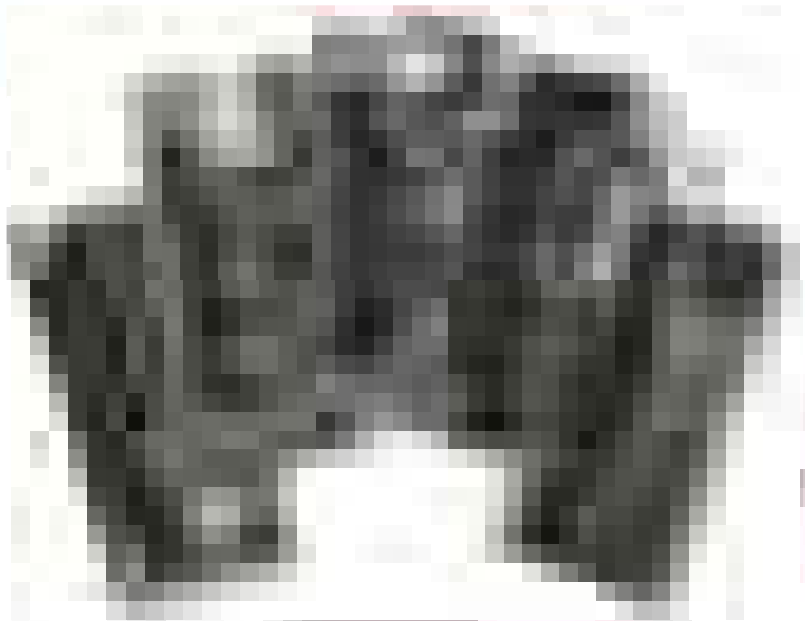


### Typical Linux kit includes:

- Target CPU card
- Preloaded OS image on 256 MB industrial CompactFlash
- 256 MB SO-DIMM module
- Interface cables
- Hard copy of manual
- Mouse
- CPU OS bootable CD
- Optimized OS version
- Full driver support for on-board hardware
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- Example applications and source code
- Extra documentation

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**XBLOKs** offer the best compromise in cost and function for both PC/IO4 and PC/IO4-Plus. Only 44% the size of a standard PC/IO4 card, you can add two functions to your system but increase the stack height by only one level. -40° to 85° C. Heat diagram shows enhanced cooling.



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- Direct connection to opto-module racks

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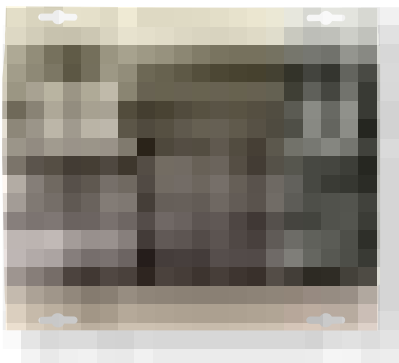
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- 10/100 Base-T, Intel 82551ER
- Fully plug-n-play
- High performance, PCI bus interface

### **X-USB-4 quad USB 2.0**

- Speeds up to 480 mbps
- Mix and match USB 1.1 and 2.0
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& other RTOS supported
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**COTS** (kots), *n.* 1. Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. 2. Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

—Ant. When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. E.g., *rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

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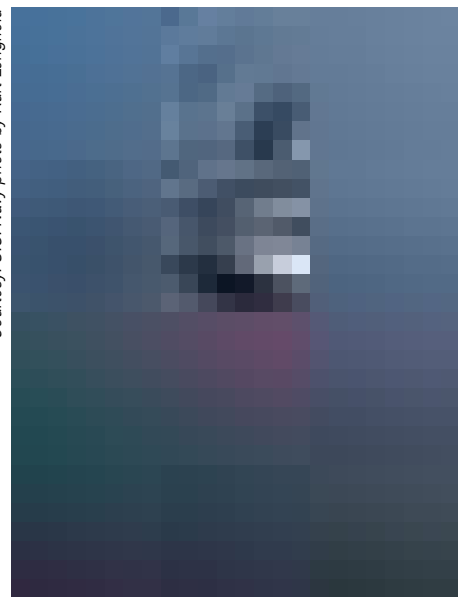
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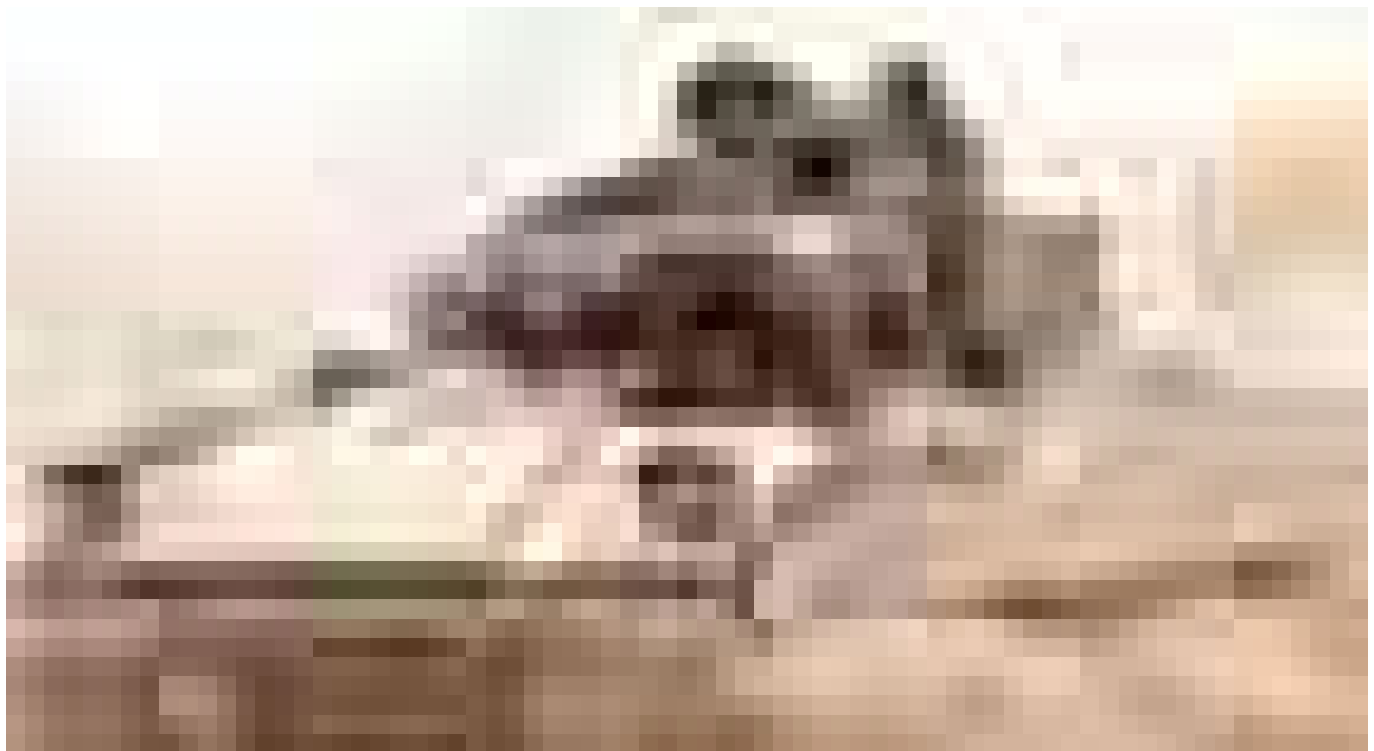
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In mid-January the Navy's RQ-8A Fire Scout tactical UAV made history performing the first autonomous landing aboard a Navy vessel at sea. The aircraft is shown here, moments before that landing, as it nears the amphibious transport dock ship USS Nashville (LPD 13). With an on-station endurance of over four hours, the Fire Scout system is capable of continuous operations, providing coverage at 110 nautical miles from the launch site. The Navy Fire Scout has a baseline payload that includes EO/IR sensors and a laser rangefinder designator.

Courtesy: U.S. Navy photo by Kurt Lengfield





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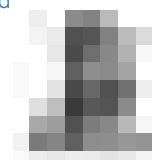
### **RM921** **VME Managed Gigabit** **Ethernet Switch with IPv6**

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### **VME-5565** **Ultrahigh Speed Fiber Optic Reflective** **Memory with Interrupts**

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- DMA controller
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- Ultra low CPU overhead, onboard hardware manages communication protocol



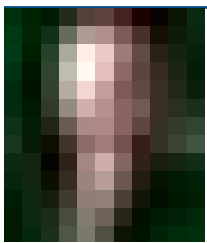
### **Sentinel** **Ruggedized Flat** **Panel Monitor**

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**Embedded Systems**

# Publisher's Notebook



## The Military Needs an “EASY” Button

In order to provide our readers with information that is relevant, we're constantly attending or participating in different industry events. Some events like ESC and MEECC are very close to what we write about, while others like MILCOM, TechNet, I/ITSEC and AUSA are more distant. An emersion in both elements of this spectrum is essential to fully appreciate the implications of the technology that we write about.

The ESC-type conferences provide focus on emerging component and subsystem technologies that are or will be part of the electronics our industry will be using. The AUSA-type conference tells us how the results of those technologies are being implemented and what technologies will be needed in the future. In February, Warren Andrews, Editorial Director; Jeff Child, Editor-in-Chief and I all went to AUSA Winter in Ft. Lauderdale, Florida (at least they know what location to select in February). We attend this conference regularly, and it's a “big iron” event: you get to see everything from armored vehicles to munitions.

On the surface it's not very apparent what benefit a publication that deals with embedded electronics obtains from a show like AUSA. I could probably do a whole white paper addressing that question. But in the space of this column suffice it to say that what you obtain is a window into the future, not from any one program but a collection of programs: How have they transitioned? Where will they go in the future? What are their critical electronic needs? Then you compare the electronics required to accomplish that to what our industry is doing and where it is going. We then throw in a pile of intuition and market experience and come up with technologies that we need to focus on in *COTS Journal*.

For the last year the computer industry has been buried in “lead-free” presentations and discussions. The problem is none of them really focus on the military market, so I thought I'd ask around the AUSA conference to find out what the “big iron” guys' thinking was on the subject. The result was scary. The responses can be reduced to three basic thoughts: It doesn't affect us, because military programs are exempt; It doesn't affect us because we build our own sub assemblies and will continue to build leaded assemblies; And, finally, this isn't an issue for us, our suppliers are handling it. In summary, no one is even considering the big picture, in other words, all the components: from a resistor to a microprocessor.

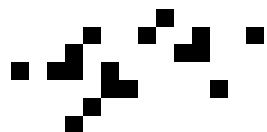
DMEA and some specialty packaging fabs may be able to help with some of the more complex pieces of silicon by producing leaded parts, but only a very limited number and no where

near all the silicon that ends up in Mil systems. Is there a plan in place to stockpile leaded electronic components for all the systems that are out there? None that I'm aware of. Yes, there is some component stockpiling but on a very limited basis. Is there going to be a mandate that components will have to be stockpiled? If so, when will it be issued and who will bear the cost?

What about boards that come back for depot or manufacturer repair or upgrade? What plan is in place to cope with mixed technologies on boards? Is there anything in current contracts regarding lead vs. no-lead, or its testing, or the liability for failures? Let me tell you, no matter who I asked, I could tell that no one had an answer and they were extremely disturbed that I even asked the questions. It's like everyone has their head in the sand when it comes to this topic. It's either that they think it just won't affect them or that this could be a financial windfall where someone will make a lot of money building custom things that are leaded.

In December 2005 the National Academy of Sciences produced a report that was provided to the DoD and Congress citing the problem that we are facing mostly with Printed Circuit Boards (PrCBs), entitled “Manufacturing Trends in Electronics Interconnection Technology.” This report alone should have everyone in Congress and the DoD very nervous (I can email you a summary). I don't know if everyone in those organizations thinks that they will be out of office when the next crisis hits—when we'll have to start a commission to see who was asleep at the switch.

The military and politicians need to accept that we are in a crisis situation and they need to take their heads out of the sand. The military component market is a niche market for component suppliers, one that they can easily ignore completely without affecting their bottom line. Innovation and leading-edge technology is moving at a lightning pace and a function of the consumer market. The military needs to harness that technology to stay ahead of the people that want to do us harm. There is no “EASY” button (I hope Staples doesn't mind me using their slogan) for the military. We need action now, not a commission to find fault when it's too late. ■■

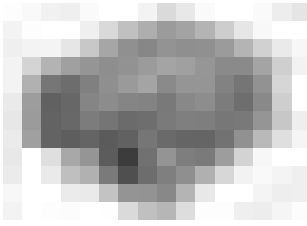


Pete Yeatman, Publisher  
*COTS Journal*

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### News Release

#### LOW POWER MONOLITHIC CMOS 3.3V MIL-STD-1553 BC/RT/MT MESSAGE PROCESSOR

*Mission Viejo, CA, Holt Integrated Circuits today announced the availability of the HI-6110, single-chip CMOS 3.3 volt MIL-STD-1553 Message Processor. The HI-6110 is a CMOS integrated circuit designed to implement the MIL-STD-1553 data communications protocol between a host processor and a dual redundant 1553 data bus, and supports MIL-STD-1553B Notice 2 and MIL-STD-1760 Stores Management.*

The HI-6110 is a single-chip protocol device and

includes on-board dual redundant transceivers as well as Manchester Encoder/Decoders, MIL-STD-1553 message-level protocol engine, and sufficient on-chip data storage for single message buffering. With exceptionally low power the device dissipates less than 500 mW on-chip power at 100% duty cycle. The HI-6110 may be configured as a Bus Controller (BC), a Remote Terminal (RT), an addressed Monitor Terminal (MT), or as a non-addressed MT. All that is needed to interface to the MIL-STD-1553 bus is an isolation transformer for each channel (also available from Holt). The host CPU communicates with the HI-6110 over a 16-bit parallel Input/Output bus. The status of message sequencing and the data transfers are flagged by pins and register bits. Registers are provided for configuration, status information, error information, and the type of the currently executing command.

The HI-6110 Message Processor introduced by Holt is the first new bottoms up design provided to the market in years. Care has been taken to provide customers only what they need, and eliminate unnecessary legacy operating modes. The HI-6110 uses system memory for 1553 message data which is configured by the user to specifically meet the needs of the application. As a result, the device can be offered in a small package that takes full advantage of the host processor / memory at a price offering significant cost savings to the system designer. The HI-6110 is offered in either a 52-pin plastic quad flat pack (PQFP) or a 60-pin plastic chip-scale package.

"Designers of military avionics data bus systems have waited a long time for a simple, fully integrated MIL-STD-1553 terminal IC that acts as a peripheral device to the system's host processor," says David Mead, Executive Vice President and COO of Holt Integrated Circuits. "The 3.3 volt HI-6110, with its exceptionally low power consumption, allows the designer to focus on their system application, and hand off the detail protocol management to the message processor."

Engineering samples of the HI-6110 PQI in the 52-pin PQFP package are now available from Holt, along with an accompanying Remote Terminal evaluation / demonstration board to customers wishing to evaluate the device for new production designs.

### News Release

#### 3.3V ARINC 429 LINE RECEIVER OFFERS EXCEPTIONAL INPUT COMMON-MODE PERFORMANCE

*Holt Integrated Circuits announces the newest of their 3.3 volt ARINC 429 CMOS products with the release of the HI-8591 and HI-8591-40 Line Receivers. The HI-8591 is a highly integrated CMOS bus interface receiver designed to operate from a single 3.3 volt or 5 volt supply. The part is designed with high-impedance inputs to minimize bus loading, and has exceptional*

*input common-mode performance in excess of  $\pm 30V$ , making it immune to ground offsets around the aircraft.*

Like other Holt ARINC 429 Receiver products, the 3.3V HI-8591 is offered in a "-40" variant to simplify the circuit design in applications where lightning protection may be a concern. The HI-8591-40 requires only the addition of external 40K Ohm resistors in series with RINA and RINB to allow the part to meet the pin injection lightning protection requirements of DO-160D, level 3.

"The demand for 3.3 volt databus products is increasing," says Jerry Donaldson, Marketing Director at Holt. "Holt is successfully implementing our strategy to expand our 3.3 volt offerings with both ARINC 429 and MIL-STD-1553 products, while continuing to support the long-term production and customer support of our industry standard 5 volt products."

The HI-8591 and HI-8591-40 are available in the very popular 8-pin plastic SOIC and an ultra-small 16-pin 4mm x 4mm LPCC Chip-scale package. Other package options in both plastic and ceramic configurations are available to meet alternative customer requirements, with temperature screening and processing from Industrial to full Military.

## A Commitment To Excellence

## A Commitment To MIL-STD-1553

**3.3 Volt COTS Products Now Available**

Over the years Holt has worked hard to become the leading integrated circuit supplier for ARINC 429 bus interface applications. Now Holt has applied this same dedication and innovation to a family of single chip CMOS ICs for the MIL-STD-1553 protocol.

Holt's new 3.3V & 5V MIL-STD-1553 products offer superior reliability, the lowest cost and the smallest package solutions for a variety of military databus applications such as smart munitions, avionics, stores management, instrumentation and test equipment.

**MIL-STD-1553 PRODUCTS NOW AVAILABLE FROM HOLT**

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- Manchester II Encoder / Decoder
- Interface Transformers (Single & Dual)

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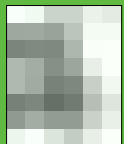
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- Linux<sup>®</sup>, Windows<sup>®</sup> and open-source eCos OS

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[www.pentek.com/go/cotsmart](http://www.pentek.com/go/cotsmart) for Pentek's "Putting FPGAs to Work for Software Radio" handbook and to request a full product catalog.



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# The Inside Track

## Boeing Demos Test Real-Time Link between Aircraft and the GIG

Boeing and the U.S. Air Force Research Laboratory (AFRL) conducted live flight tests recently to demonstrate airborne platforms acquiring, sorting and exchanging real-time mission data with each other and with command and control centers on the ground. Phantom Works engineers and the AFRL demonstrated the new capabilities on Feb. 1 and 3 during flight tests in St. Louis involving the Boeing F-15E1 Advanced Technology Demonstrator, which was modified with intelligent software agents. The software agents allow aircraft to fully exchange information in real time with the Global Information Grid (GIG)—the DoD's expansive network-centric information system. The F-15E was linked to the GIG as its aircrew flew tactically relevant scenarios similar to those flown during Operation Iraqi Freedom. It was the first time an in-flight tactical aircraft had been linked to the GIG to provide unprecedented situational awareness.

As the intelligent software agents autonomously sorted and filtered information, the F-15E aircrew quickly and accurately

sent and received only the most pertinent mission data and images along the GIG. The agents transformed Link 16 data such as target status, vehicle health, fuel status and weapon stores into information that was shared across the GIG for use by commanders in a Command and Control Air Operations Center. In turn, the commanders used this information to direct and redirect the F-15E aircrew to engage primary and secondary targets. The F-15E aircrew exercised on-demand access to the GIG for updates on friendly forces, unmanned air vehicles

and intelligence, surveillance and reconnaissance data around target areas. Boeing Phantom Works has been under contract with the AFRL since October 2004 to develop information management services that provide network-centric machine-to-machine interoperability between tactical fighters and command and control elements.

Boeing Phantom Works  
Seal Beach, CA.  
(562) 797-2020.  
[[www.boeing.com](http://www.boeing.com)].



Figure 1

Two Air Force F-15 Eagles are shown flying in formation over the Atlantic. The Eagle is an all-weather tactical fighter designed to gain and maintain air supremacy over the battlefield. Boeing and the AFRL used an F-15E1 Advanced Technology Demonstrator version of the F-15 for the demo. (U.S. Air Force Photo).

## CMC Electronics Picks Green Hills Software Platform for Avionics

CMC Electronics, the Canada-based designer of aviation and global positioning systems, has chosen a Green Hills Software Platform for Avionics for its Flight Management Control

and Display (FMCDU) system. The platform consists of the INTEGRITY-178B real-time operating system (RTOS), GSTART Ravenscar-compliant Ada kernel and AdaMULTI development environment. CMC will also use the set of software for the development of its Electronics Aircraft Management System

product line, which is based on a PCI open system architecture.

INTEGRITY-178B is a time and memory partitioned operating system, certified to DO-178B Level A with full ARINC-653-1 compliance.

Support for ARINC-653-1 with its partitioning definition allows developers to deploy multiple applications on a single processor, at potentially multiple safety certification levels. That allows developers to reduce the number of onboard computers needed to support multiple software systems. The Platform for Avionics with INTEGRITY-178B is certified for multiple languages, including: Ada, C and Embedded C++.

Green Hills Software  
Santa Barbara, CA.  
(805) 965-6044.  
[[www.ghs.com](http://www.ghs.com)].

## Carrier Selects Teledyne Controls' Avionics Gear for its A320 Fleet

Air One, the second largest airlines in Italy, has chosen to install Teledyne Controls' FDI MU (Flight Data Interface Management Unit) and Wireless GroundLink (Wireless Quick Access Recorder - WQAR) on its new aircraft fleet. The Italian carrier, which recently purchased 30 A320s, with 60 more on option, will use Teledyne's equipment to fully automate the acquisition, recording and transmission of its flight data. The FDI MU will enable Air One to collect mandatory and ACMS data from the aircraft, while Teledyne's Wireless GroundLink will fulfill the data recording function, along with the secure and seamless transmission of the data to the ground.

Teledyne Controls' FDI MU is a compact and integrated data



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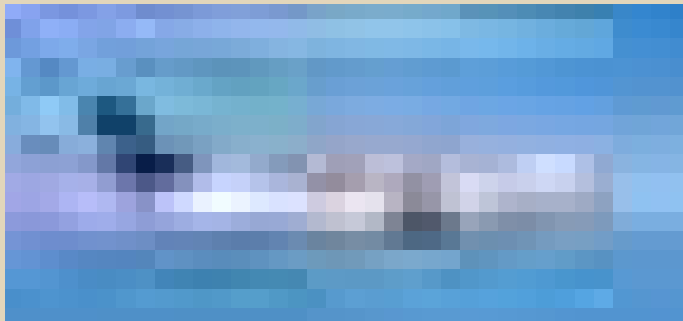


Figure 2

Italian carrier Air One will install Teledyne Controls' Flight Data Interface Management Unit and Wireless GroundLink system on its new fleet of recently purchased Airbus A320s aircraft.

acquisition and recording system available for installation on the Airbus Single Aisle A319/A320/A321 and Long Range A330/A340 aircraft families. Based on Teledyne's concept of LRU Compression, the FDIMU combines into a single Line Replaceable Unit (LRU) the multiple functions of traditionally separated systems. The Wireless GroundLink is designed to automate flight data recording and transmission, and therefore reduce data delivery delays and risk of data loss involved with traditional manual procedures. The GroundLink system can record and wirelessly transfer flight data from the aircraft to the ground, without any human intervention. Using a proprietary protocol patented by Teledyne, the raw data recorded during flight is compressed, encrypted and then transmitted via cellular technology and the Internet to the airline's or Teledyne's ground-based data center for processing and analysis.

Teledyne Controls  
Los Angeles, CA.  
(310) 820-4616.  
[www.teledyne-controls.com].

### TTTech and LynuxWorks Team for Deterministic Avionics Comms Solution

TTTech and LynuxWorks have formed a partnership to offer customers integrated solutions based on the deterministic TTP communication bus and the LynxOS DO-178B-certified RTOS. A new TTTech development board for hardware-in-the-loop simulation of aerospace test equipment, which supports simulation of a whole distributed network for aerospace applications with hard real-time

requirements, will be the first project to benefit from the partnership. The TTTech TTP (Time-Triggered Protocol) bus is a bi-directional, partitioned and fault-tolerant databus that offers deterministic performance up to 25 Mbits/s. LynuxWorks LynxOS-178 features DO-178B level A certification, partitioning, POSIX compliance and ARINC 653 Application EXecutive (APEX) support. Both address very directly the stability and standards compliance expectations of military and aerospace system developers seeking to build safety-critical, certifiable applications.

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San Jose, CA.  
(408) 979-3900.  
[www.lynuxworks.com].

TTTech Computertechnik  
Vienna, Austria.  
+ 43 1 5853434-0.  
[www.tttech.com].

### NASA Taps VPT for Power Systems in Multiple Programs

The National Aeronautics and Space Administration (NASA) has awarded a contract to mil/aero power conversion vendor VPT for research and development of power systems for use in multiple future space vehicles and systems. Under the terms of the contract award, VPT will design and build prototype power systems for multiple NASA power system applications. Each system will be created using a modular—and therefore cost-efficient—component approach with VPT DC/DC power converters and EMI filters serving as the base for the system. All resulting power systems will meet stringent NASA requirements for design, parts selection, element evaluation, screening, radiation hardness and qualification.

Targeted NASA uses for the new power systems from VPT include the NASA-JSC Space Station applications including power converters for the IBM A31 Notebook Computer PC used by astronauts, as well as a power system for the James Webb Space Telescope (JWST) (Figure 3). The contract also includes a power system for the CEV and lunar orbiter and a space-borne GPS receiver for attitude and orbit determination. VPT expects engineering units developed under this contract award to be available to prime contractors in approximately six months, with full scale production units available by the end of 2006.

VPT  
Blacksburg, VA.  
(540) 552-5000.  
[www.vpt-inc.com].

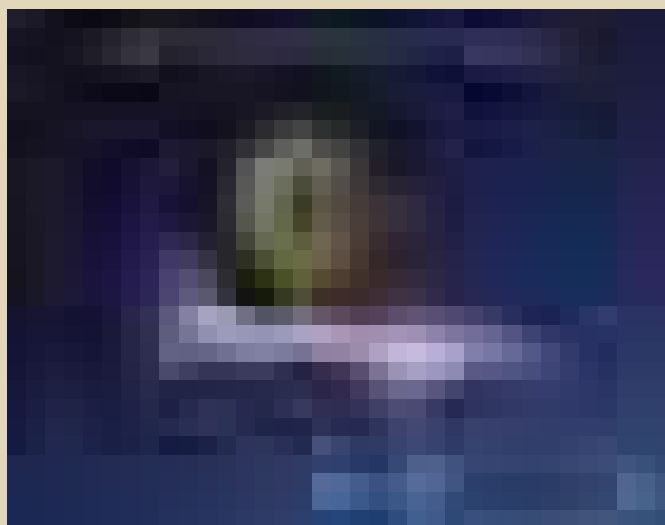


Figure 3

Scheduled for launch in 2011, the James Webb Space Telescope (JWST) is a new, larger successor to the Hubble Space Telescope. Shown here is an illustration of the JWST as it will be deployed. The gold-coated telescope mirror is shown at the top of the picture, the purple sunshield at the bottom.

## COTS Websites

[www.equipment-reliability.com](http://www.equipment-reliability.com)

### ERI Website Educates on Rugged Test

Reliability and durability rank high among the priorities of military and aerospace system designers. The Equipment Reliability Institute specializes in just such information. ERI's site has developed into a fount of knowledge, a listing of resources and a place where engineers can come for information and assistance concerning reliability and durability of systems. ERI is an affiliation of engineers dedicated to increasing the reliability and durability of automobiles, aircraft and other vehicles, as well as electronic and other equipment. ERI develops and presents technical education to help lessen or avoid immediate and future reliability and durability problems. ERI also offers consulting services for any specific and



immediate reliability and/or durability problems, this activity is called ERG or Environmental Reliability.

ERI offers training programs: open courses, onsite courses or a special Distance Learning Program. Articles and presentations on a variety of reliability related topics can be found on the site, such as climatic and dynamic testing, ESS, HALT, HASS and long-term reliability testing. For specific shock and vibration issues, ERI also maintains [vibrationandshock.com](http://vibrationandshock.com).

Equipment Reliability Institute (ERI), Santa Barbara, CA.  
(805) 564-1260. [[www.equipment-reliability.com](http://www.equipment-reliability.com)].

### PowerNode5: the rugged blade server that keeps you on the cutting edge.

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server and easily deployed on the PowerNode5 system. What's more, thanks to the smooth migration path from PowerPC AltiVec™-based platforms as well as a software insulation layer common with previous versions your legacy software investments are preserved. Choose between board component versions (the PowerNode5) or the pre-integrated PowerMP5. Transport and management software are standards-based and both products run Red Hat Linux or Wind River VxWorks. No wonder more blue-chip companies are turning to ruggedized solutions from Thales Computers to meet their critical computing needs.

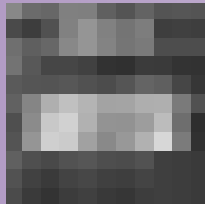


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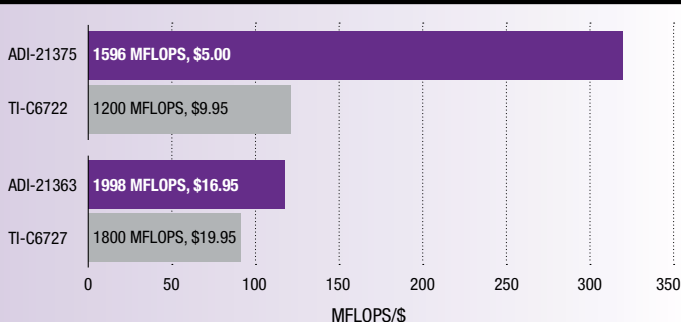
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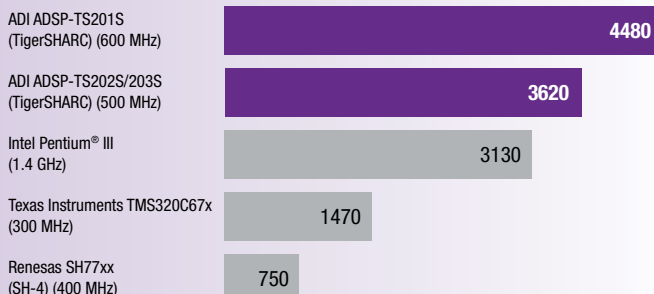
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— Dr. Alan Oppenheim  
Ford Professor of Engineering  
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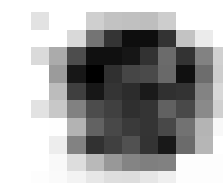
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# Program Briefing

Joint Tactical Radio System

## JTRS Program Wrestles with IP and ITARS Conundrums

Challenges lay ahead for JTRS as the troubled program sorts through critical issues

Jeff Child

**C**harged with the goal of meeting diverse warfighter communications needs through software programmable radio technology, the DoD's multi-services Joint Tactical Radio System (JTRS) represents one of the most ambitious and technically challenging programs ever conceived. It's a central element of the military's plan for Network Centric operations using seamless real-time communications including voice, data and video—with and across the U.S. military services, and with coalition forces and allies (Figure 1).

Like many other complex programs, JTRS, not surprisingly, has been faced with product delays and cost overruns, and last year the JTRS Program went into reorganization mode. Today, almost a year later, the results of that have yet to be announced. There was talk of a resolution last fall, but now observers are saying that it will be March before we hear anything about Clusters 1 and 5, and maybe as late as June for AMF. Meanwhile, Congress has made significant cuts to the JTRS budget, which might well explain the delays in hearing from the JTRS JPEO. And while

development and prototype work continues, it's becoming clear that there are some fundamental problems—some not technology-related—that, unless solved, will prevent JTRS from moving forward.

The most significant problem is the rocky transition from the old business model for creating military radios to the JTRS model, which calls for the sharing of software radio waveforms capable of running on any JTRS SCA-compliant radio. In the old model, a company that won the contract for a radio would own more or less all the Intellectual Property (IP) comprising that radio. If you required

a radio with the Enhanced Position Location Reporting System (EPLRS), for example, Raytheon would make and sell the radio because they own the EPLRS waveform.

### New Business Model

In contrast, JTRS—and software defined radios in general—turn that model upside down. For JTRS development there's a repository of waveforms where anyone who needs the waveform because of the government contract, can go in and get it for free. That poses a problem because now companies who develop waveform IP are essentially more or less being asked to provide it for free.

That's a major issue and it's causing a lot of conflict in the industry. And, to date, there's very little available in the repository that developers can make use of.

A recent example is Soldier Radio Waveform (SRW), which is being used by JTRS Cluster 5. SRW started out as a DARPA program called Small Unit Operations Situational Awareness System (SUO/SAS), and as such was initially DoD funded, and the government owned the IP. Since then, ITT Industries,

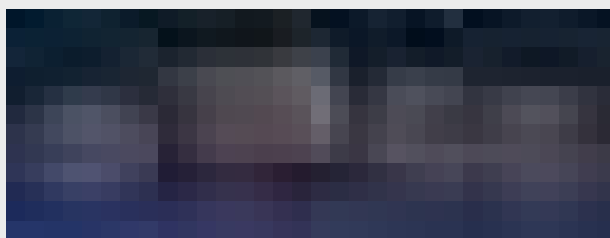


Figure 1

These prototype JTRS Cluster 1 radios are designed to provide secure capabilities, including real-time voice and text transmission/receipt, live video and audio streaming, drawing and sharing of maps, Net-Meetings and Voice over Internet Protocol (VoIP). Source: Boeing.

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along with third-party partners, invested R&D into making it a networking waveform and making power efficient. ITT Industries owns the IP for SRW, and they are not providing source code for that IP. That means that radio makers that need to run SRW, can't get access to it. There's no incentive for developers of waveforms, like ITT, to give them away

for free. Unfortunately, there's no business model or license fee structure set up within the JTRS Program to regulate that access. The Wideband Networking Waveform (WNW) is another example. So far the only specifications available for WNW are specific to Boeing's implementation of WNW.

### SCA Fails to Gain Commercial Acceptance

Aside from the lack of an IP business model, the other major problem facing JTRS is the failure of the DoD's Software Communications Architecture (SCA)—the core software architecture for JTRS—to get any traction as a commercial standard. One of the objectives right from the start for the JTRS program was to entice the broad software radio market to accept the SCA standard. The hope was that SCA would be embraced by commercial wireless infrastructure vendors—like Ericsson, Nokia, Nortel and the like. That would bring costs down by leveraging commercial SCA-compatible offerings available in the market—all the standard COTS arguments.

Because those wireless infrastructure giants are keen on selling base stations, they've been reluctant to move to any kind of open source model for the software in those base stations. Even if they did, there's one particular hurdle that makes SCA a problematic choice for any non-U.S. firm. The SCA 2.2 spec—the current spec mandated by the JTRS program—doesn't specify how to interface waveform components within devices like DSPs and FPGAs. The way that's been handled in JTRS Cluster 1 radios is through a hardware abstraction layer called M-HAL. Boeing owns the M-HAL spec; it is currently ITARS (International Traffic in Arms Regulations) restricted so it can't be used by non-U.S. citizens. With such hurdles in place, there's little hope that SCA could practically be used by the commercial market.

Until the IP and ITARS issues plaguing JTRS are ironed out, it's unlikely that the program will be able to move forward. And because many other DoD programs depend on JTRS, these problems are likely to cause a lot of controversy. The most recent ORD for the Future Combat Systems program, for example, actually changed the wording to be more generic in its reference to radios. Originally, the JTRS Cluster 5 radios were to be the FCS radio, but now FCS program managers are not limiting themselves to that. That seems to be a way of saying, "We'll see what's available for radios, but if JTRS isn't working that's not going to stop us from using another radio." ■■

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# Main Feature

Switched Fabrics: Military Update

Coming in April  
COTS Journal-VME for  
the Next 25 Years : Part II

## VME for the Next 25 Years: Part I, Switched Fabrics Entrench with VME

Never a community keen on embracing change for change's sake, the military market has been cautious about serial switched fabrics. That resistance is thawing as fabrics blend with VME form-factors and into nearly every level of standards-based embedded computing.

Jeff Child

There's no doubt that the board-level embedded computing community has excelled in its ability to develop and productize technologies critical to the military market—and do so long before military system designers know what they want or need. Serial switched fabrics are a perfect example along those lines. Switched fabric technologies have been around for several decades in niche, high-end embedded applications. But even when they started to migrate into the mainstream embedded computing realm around six or so years ago, the military market expressed absolutely zero interest in them, and for good reason.

Given the decades-long design cycles in the defense arena, it's too risky to take any long-term development project on an interconnect scheme that won't be around in a few years. Indeed, most of the current VME systems deployed use the traditional VME64. On the other hand, the inherent performance limitations of parallel buses like ordinary VME64 and PCI, telegraphed an eventual shift toward serial fabrics.

Fortunately the VME community started the ball rolling a couple years ago on the underlying spec development to bring serial switched fabrics into the VME

space. Among those standards currently under development are VITA 41, VITA 42 and VITA 46. VITA 41 (VME Switched Serial or VXS) is an evolutionary draft standard that enhances the existing parallel VMEbus to support switched fabrics while maintaining backward compatibility with existing VME backplanes. VITA 42 (Switched Mezzanine Card or XMC) is an evolutionary draft standard that adds high-speed interfaces to existing PMC mezzanines to support multiple high-speed fabrics while retaining compatibility with existing PMC sites.

VITA 41 (VXS) and VITA 55 (Virtual Streaming Protocol), are two of the “here and now” switched fabric approaches that marry fabrics and VME. VITA 55 implements a low-overhead point-to-point link between FPGA-based endpoints and can be used on a variety of physical layers. For more details on VITA 41 and VITA 55, in the context of military signal processing applications, see the article “Switched Fabric Schemes Enable Right-Sizing to an Application” on p.36 in this section.

Meanwhile, another spec, VITA 46, promises a more revolutionary upgrade to military subsystem architectures with high-speed switched serial backplanes that support Advanced Switching Interconnect (ASI) and Serial RapidIO. VITA 46 is suited for connecting multiple processors, peripherals and I/O cards within chassis. The article “ASI Makes a Compelling Choice as Military Embedded Fabric” on p.31 in this section discusses

the merits of blending ASI and VITA 46 for next-generation requirements.

### Here a Fabric, There a Fabric

The VME realm isn't the only arena where switched fabrics are making a presence. Last year was a busy year for switched fabrics—PCI Express in particular—across all areas of standards-based mid- and high-embedded architectures. Table 1 lists the various board-level form-factors that are employed switched fabrics. Targeting the military market specifically, PICMG approved the CompactPCI Express spec this summer. Making use of the same connector specified for ATCA, it provides a migration path for designers who use the CompactPCI form-factor but want the added performance of PCI Express. The specification defines the connector, electrical and mechanical requirements of 3U/6U system boards, peripheral boards, switch boards and backplanes.

PICMG also brought the Computer-On-Module (COM) Express spec under its wing. COM Express is an architecture for integrating all components necessary for a bootable host computer, packaged as a super component. Interfaces will provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the move from PCI bus and parallel ATA to PCI Express and Serial ATA. The PC/104 community stepped into the world of switched fabrics with its new EPIC Express spec.



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# Main Feature

Switched Fabrics: Military Update

## Switched Fabrics Play Well in Data-Centric Systems

Large-scale networked applications, like shipboard nets, push the limits of traditional distributed architectures. A blend of switched fabric hardware and publish-subscribe software helps smooth the way.

Dr. Rajive Joshi, Principal Engineer, Real-Time Innovations

Improving performance is a perennial system design goal for military system developers. When designing distributed systems with thousands of nodes that need to move a lot of data around quickly, achieving adequate performance becomes much harder. Fortunately, publish-subscribe systems that use a switched fabric for networking have proven that they can perform better than other distributed architectures in even the most demanding situations.

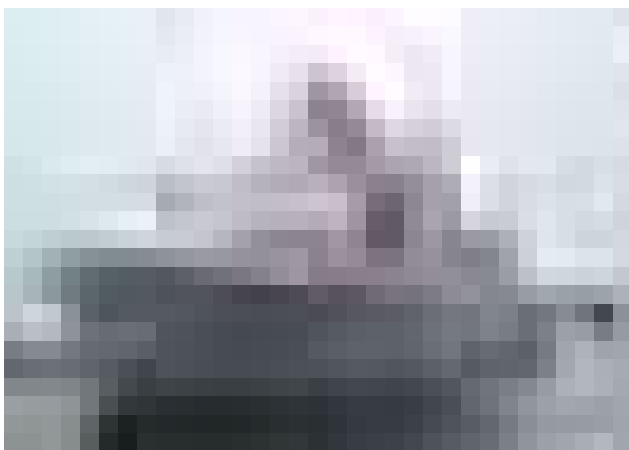


Figure 1

The USS San Antonio (LPD-17) uses RTI's NDDS middleware as the backbone for its Ship-Wide Area Network (SWAN). The ship is shown here departing Pascagoula, Mississippi last December.

Many modern large-scale applications can be characterized by three attributes: they need to gather and distribute data in real time; the amount of data being transferred is significant; and the entities involved in this data exchange are varied and may even change over time. Example applications along those lines are air traffic control and battlefield or naval command and control. The U.S. Navy's new LPD-17 Amphibious Transport (Figure 1), (the USS San Antonio), uses a distributed data-centric scheme to form the backbone of its entire Ship-Wide Area Network (SWAN).

The data-centric architecture flattens information or data distribution patterns, making data sources directly available to any authorized node on the network that wishes to use the data (Figure 2). Applications, once centralized on high-performance servers, can now be disaggregated and decentralized to span multiple networked computers. Disaggregated or distributed systems are much easier to scale, make fault-tolerant and upgrade. This disaggregation calls for new application infrastructures.

Publish-subscribe communications and switched fabrics are key enablers of these new distributed architectures. Data sources publish their data to the network; data users subscribe to the data to receive real-time updates. This data-centric transformation is revolutionizing embedded and real-time system design. Switched fabrics replace bus backplane and serial interconnect technologies. StarFabric, PCI Express Advanced Switching, Serial RapidIO and InfiniBand are the leading switched fabric schemes that are available today.



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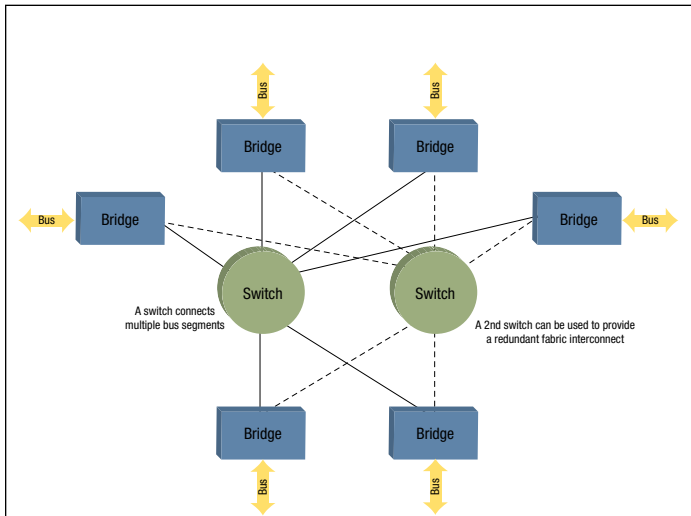


Figure 2

Switched fabric technology enables a node to communicate with any other node at speeds comparable to that of the local bus. A redundant fabric may be used for hardware fault tolerance.

### Publish-Subscribe Scale for Switched Fabrics

A key characteristic of switched fabrics is that they allow peer-to-peer communication between nodes without having to physically connect every node to every other node. With every node connected to every other node, adding a new node is exponentially more and more expensive, the greater the number of nodes. Publish-subscribe systems do not suffer from this lack of scalability.

On the software side, publish-subscribe communication systems map very naturally onto switched fabrics. The entities in publish-subscribe systems are also peers—they directly communicate with each other, so the topology of publish-subscribe systems can be closely matched to that of switched fabric systems. In other words, publish-subscribe systems are naturally scalable.

Publish-subscribe systems are also good at real-time data distribution, they are more easily field-upgradeable, and they are transport- and topology-agnostic. They are better at real-time data distribution because they are more efficient than client-server architectures in both latency and bandwidth for periodic data exchange. They are easier to upgrade in the field because publishers and subscribers do not care who or how many their counterparts are,

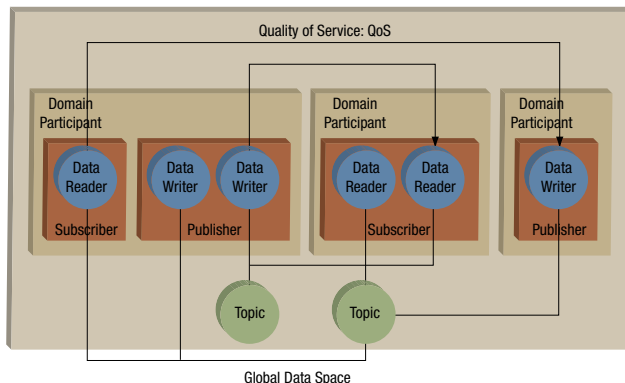


Figure 3

The Data Distribution Service (DDS) Standard uses a publish-subscribe communication model. Topics associate Data Writers with Data Readers and establish a logical communication path between them. Quality of Service (QoS) can be specified per Topic, Data Reader, Data Writer, or a combination. Publishers (Subscribers) are used to group Data Writers (Readers), and additional QoS may be specified on a per group basis. Publishers and Subscribers belong to a Domain Participant; together the DomainParticipants define a communication domain. A node on a distributed system may contain one of more DomainParticipants.

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except that they meet the Data Distribution Service standard. And finally, since publish-subscribe systems are layered on top of the physical means of getting the data from one place to another, they don't care what network transport or topology is used (Figure 3).

## DDS and Fabrics: A Synergy of Features

This marriage of switched fabrics and publish-subscribe systems offers architects new flexibility in adding capabilities that were once much harder to achieve. Many of the features offered by switched fabrics have counterparts in the DDS-compliant middleware (Figure 4).

**Error Management.** Switched fabrics typically offer rich error management features such as the ability to recognize, report and route around failed paths. With DDS-compliant software, system designers can also take advantage of DDS error reporting facilities. For example, subscribers can set the Deadline QoS policy to be notified when data is missing.

**Redundancy.** A key feature of switched fabrics is support for multiple paths between nodes. This gives system architects the ability to implement simple multiple physical interconnects that can be combined with sophisticated error management. Likewise, applications can take advantage of redundant publishers that have different "strengths." When a higher strength publisher fails, a lower strength one is automatically switched in by the DDS middleware.

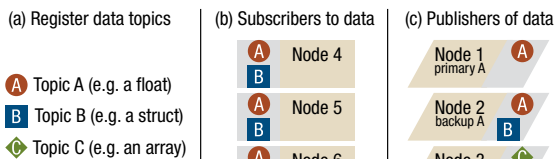
**Hot Plug/Hot Swap.** Switched fabrics specifications already provide for a hot-plug or hot swap-capability. This

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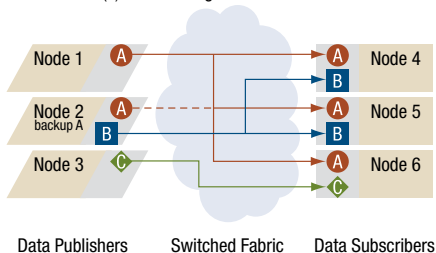
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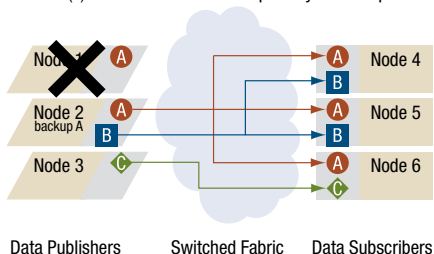
Topics identify data objects that will be sent and received. Subscribers register Topics with the middleware they wish to receive. Publishers register Topics with the middleware they will send or publish. The order does not matter.

(d) Data flowing across the network



Notice that Subscribers to Topic A do not receive data from the backup publisher on Node 2.


(e) Automatic failover from primary to backup



Example: Application on Node 1 crashes. Pub-Sub middleware automatically switches to Topic A publisher on Node 2. The subscribers get uninterrupted data.

Figure 4

DDS publish-subscribe middleware over switched-fabrics is a natural fit for high-performance data-centric distributed systems. Publishers send data directly to subscribers efficiently. Since subscribers receive data based on its name (topic) only and not on a fixed address, you can have backup publishers to achieve robust failover scenarios.



# Sometimes, flexibility is what it takes to win

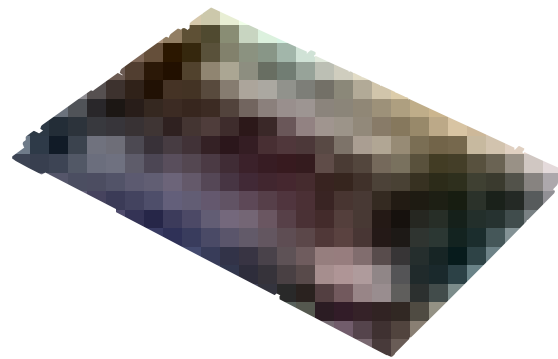
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### Radstone CP1A.

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...publish-subscribe systems that use a switched fabric for networking  
have proven that they can perform better than other distributed architectures  
in even the most demanding situations.

hardware capability can be combined with a “virtual” hot-plug capability at the application level. Unlike connection-based communication systems, publish-subscribe systems use anonymous messaging, so subscribers can be added or removed with no effect on publishers, and vice versa.

**Quality of Service.** Switched fabrics like StarFabric or PCI Express AS provide some quite sophisticated features that allow, for instance, bandwidth-reserved, isochronous transactions across the fabric, something that is not supported by, say, Ethernet. Corresponding to the hardware QoS facilities, DDS-compliant middleware offers a number of QoS policies that make predictability at the application level possible. For instance, the TRANSPORT\_PRIORITY policy allows developers to manage how they prioritize one data flow over another.

### Putting Data Front and Center

Data-centric design is emerging as a key tenet for building advanced systems where participants are distributed, interactions are data-centric, data is critical, computation is time-sensitive and storage is local. Using switched fabrics with DDS-compliant middleware is a natural design fit for such systems, providing modular scaling and giving system architects new flexibility. Now DDS-compliant real-time middleware can run on a variety of transports including switched fabrics, and provides a high-performance solution for data distribution that can be tuned to utilize the underlying fabric capabilities and deliver the needed quality of service.

Network Data Distribution Services (NDDS) 4.0 from Real-Time Innovations (RTI) is a DDS-compliant implementation. Two new features are notable: pluggable transports and new QoS policies. In addition, RTI has paid special attention to the details of implementation in order to enhance performance. The idea behind pluggable transports is to allow different physical networks to be slid in underneath the application and NDDS without requiring any change to existing code. Of course, the performance of the system may change, but the substitution itself is transparent to the application. As systems are redeployed in increasingly larger and larger configurations, pluggable transports make upgrading to larger and faster transport mechanisms as painless as possible for the application developer.

RTI has added a number of tunable QoS parameters to NDDS that are not in the DDS standard to allow a developer

to optimize their different use cases. These parameters are tunable independently for each publisher or subscriber so that an application can tune each reader and each writer for the best performance. ■■

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# Main Feature

Switched Fabrics: Military Update

## ASI Makes a Compelling Choice as Military Embedded Fabric

Armed with PCI Express as its physical layer, Advanced Switching Interconnect offers a feast of features well suited for advanced military embedded processing needs.

Stewart Dewar, Product Marketing Manager  
Curtiss-Wright Controls Embedded Computing

There's no doubt that today's backplane interconnect for mil/aero embedded computing is typified by VME and



Figure 1

Applications like the Predator UAV are hungry for multi-Gbyte/s data rates for both processor-to-processor and processor-to-I/O communications. Shown here, an Air Force sensor operator controls the RQ/MQ-1 Predator UAV's cameras from his seat on the ground. (US Army photo)

CompactPCI as the primary interconnect, with various "appliqué" methods such as Raceway or StarFabric used to provide high-bandwidth data movement when necessary. That familiar picture is beginning to shift with the emergence of open standard, high-performance serial switched fabrics such as Advanced Switching Interconnect (ASI), which can be cost-effectively integrated into standard processor cards.

That trend promises a new era of serial switched backplanes that provide multi-Gbyte/s data rates for both processor-to-processor and processor-to-I/O communications. This ultimately enables mil/aero systems such mission computers and sen-

sor processing systems to be produced at less cost and with reduced size, weight and power than with previously available technology. An example application with such requirements is the sensor processing in the Predator UAV (Figure 1).

Amongst the many serial switched fabrics available today, ASI is unique in providing PCI Express (PCIe) interoperability, which enables a wide range of system configurations to be based on a common architecture at the module level. This is only one of the many characteristics of ASI that make it a compelling choice for mil/aero embedded computing.

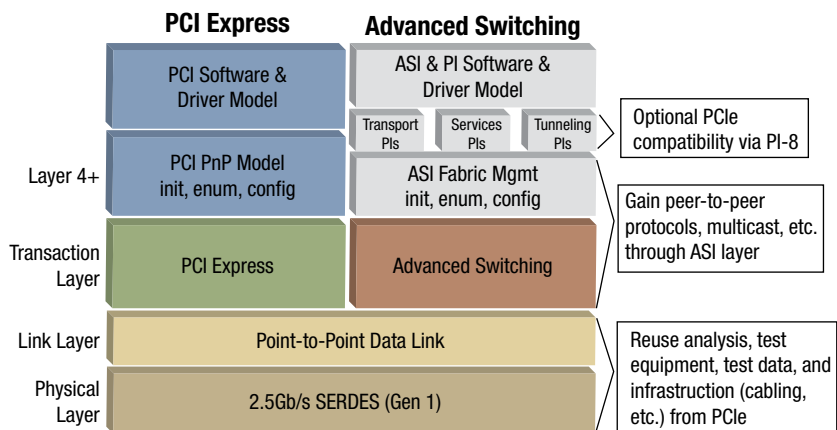


Figure 2

Advanced Switching Interconnect (ASI) extends PCI Express (PCIe) by adding peer-to-peer protocols and multi-casting.

Main Feature

An Extension of PCI Express

ASI is an extension of PCI Express that adds additional protocols to support reliable and efficient peer-to-peer com-

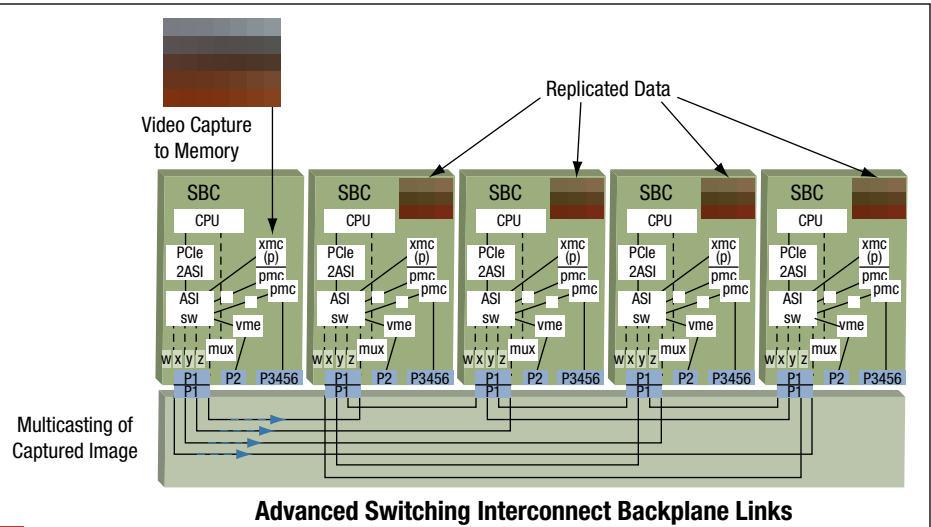
munications. The ASI suite of specifications is the work of the Advanced Switching Interconnect Special Interest Group ([www.asi-sig.org](http://www.asi-sig.org)). Due to its roots in

PCIe at the physical and logical protocol levels, the ASI serial switched fabric shares many of the performance, scalability and system integrity features of PCIe. Table 1 lists those features.

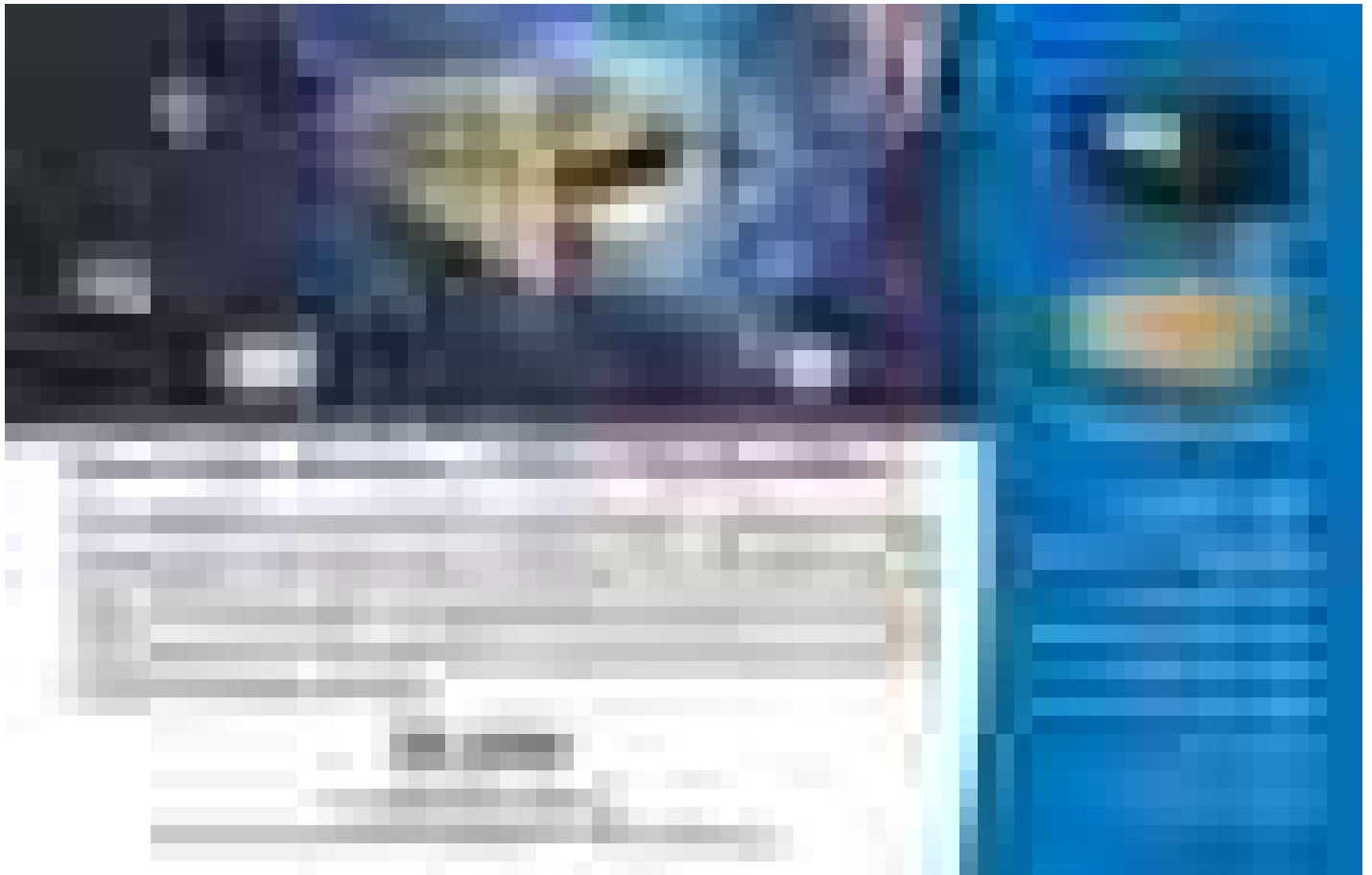
Performance, scalability, end-to-end reliable transport in hardware without software intervention, and reduced power and EMI are all features relevant to the mil/aero embedded computing environment as well as to the commercial computing environments for which PCIe was primarily architected.

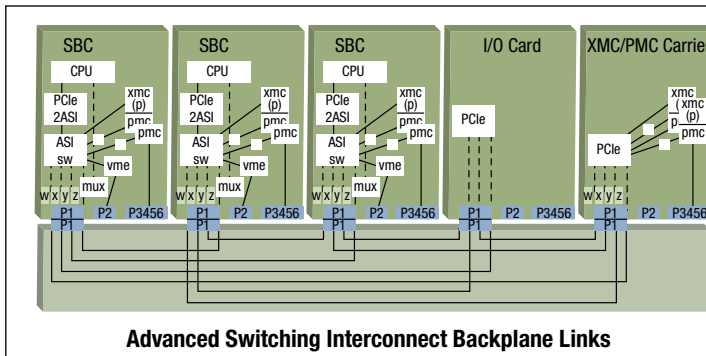
The long list of advanced features built into the PCIe foundation of ASI is a testament to the determined efforts put into the PCIe specification to make it a highly effective serialized version of the well-known conventional PCI standard that has been the dominant processor-to-peripheral chip interconnect for over a decade. What was a non-goal of the PCIe effort, however, was to address requirements for peer-to-peer communications in multi-processor systems—that is the domain of ASI.

As illustrated in Figure 2, ASI adds a



**Figure 3**  
Shown here are processor cards in a mesh communicating with ASI. One card is multi-casting captured video data to the others.





**Figure 4**

This system block diagram illustrates the use of ASI ports for both CPU-to-CPU communications and CPU to I/O communications.

highly capable protocol layer on top of the physical and data link layers of PCIe to provide a rich switched fabric capability that includes a number of useful features. It supports multiple peer-to-peer communication models such as load/store, datagram-style queues and socket-like RDMA. Flexible topologies are supported like point-to-point, star, dual-star, full mesh and cascaded partial meshes. Also provided is support for multi-casting, redundant paths and failover mechanisms. There's also a comprehensive error reporting system allowing all errors to be reported to one centralized management entity. And, finally, ASI has the ability to carry standard PCIe traffic through what is referred to as Protocol Interface 8 (PI-8) mappings.

Figure 3 shows a system comprised of multiple processor cards communicating over ASI in a mesh configuration and illustrates how multi-casting can be used to speed the dissemination of data to the processing elements. Thanks to its optional PCI Express (PCIe) interoperability, the Advanced Switching Interconnect fabric provides an interface to switched serial backplanes that can be either used as a fabric in its native ASI mode, or as a PCIe extender for connection to I/O cards and/or PMC/XMC carrier cards.

That dual-mode capability provides mil/aero system integrators great flexibility in how they employ ASI-based single board computers—making use of native ASI backplane ports when processor-to-processor connectivity is required and using the PCIe mode of operation when I/O expansion is required. Figure 4 shows a mixed system of processor cards, a PCIe I/O card, and a PMC/XMC carrier card, which illustrates the flexibility derived from the PCIe interoperability of ASI.



Main Feature

Additional system flexibility is derived from the fact that ASI can be directly carried over a cable up to 7 meters long, or over a multimode fiber-optic cable by connecting the ASI signals to a standard 4-channel parallel fiber-optic transceiver. Transmitting ASI over a cable provides a number of options to the mil/aero systems integrator. It could, for instance, provide a redundant link between primary and

backup mission computers—an application that would take advantage of the failure reporting and failover capabilities defined in the ASI protocol. ASI also makes sense as the link between a main sensor data processor positioned in an aircraft's equipment bay and a front-end data acquisition unit located in a space-constrained location close to the actual sensor. In both cases, having ASI

acting as both the core interconnect and the inter-system communication link has the advantage of avoiding data conversions that require special hardware (thus increasing space, weight and power consumption) and associated software drivers.

Enabling ASI in Mil/Aero Environments

Today's PCIe and Advanced Switching Interconnect devices have signaling rates of 2.5 Gbits/s and "generation 2" devices on the horizon will work at 5.0 Gbits/s—both these rates are well above what the connectors used on VME and CompactPCI cards can handle with acceptable levels of electrical insertion loss and cross talk. Thus using ASI as a back-plane interconnect requires the use of a newer, more capable connector type, as



Key Features of Advanced Switching Interconnect	
✓	2.5 Gbit/s signaling rate per differential Tx and Rx pair (called a lane), yielding a nominal data rate of 250 Mbytes/s in each direction per lane
✓	An ASI port can have 1, 2, 4, 8, 16 or 32 lanes, for a maximum potential data rate of 8 Gbytes/s per port in each direction, or for a more typical 4-lane port, 1 Gbyte/s in each direction
✓	8B/10B encoding and end-to-end packet CRC
✓	Reliable data transport with hardware-based ACK/NAK protocol with automatic packet retransmission on errors
✓	Signaling waveform incorporating pre-emphasis/de-emphasis that extends the path length over which the signal can be reliably transmitted and recovered
✓	Prioritization of data flows ("quality of service")
✓	Physical layer supports bit scrambling to reduce EMI (eliminates long sequences of 1s or 0s that create a square wave)
✓	Support for spread spectrum clocking, which further reduces EMI
✓	Power management provisions that automatically put the physical level transceivers into a low-power state if there is no data traffic

Table 1  
Listed here are the major advantages of the ASI fabric, many of which are shared with PCI Express.

does the use of other serial interface types that might be taken to the backplane such as Serial RapidIO, Serial ATA and Serial Attached SCSI for storage, high resolution digital video and FPGA serial interconnects such as Xilinx' RocketIO. For this reason a number of leading mil/aero board and subsystem suppliers formed a working group within the VITA Standards Organization (VSO) to standardize the new VITA 46 module format, also known as VPX.

Key attributes of the VPX module format include both 3U and 6U options defined; the 6U option retains the familiar 6U mechanical format of VME and 6U CompactPCI, and the 3U option is based on 3U CompactPCI mechanicals. Both air- and conduction-cooled formats are defined. For connectors, VPX specifies the Tyco 7-row MultiGig RT2, which is compatible with data rates up to 6.25 Gbits/s. A 6U module, the connector provides a total of 464 signal contacts and over 200 ground contacts, and up to 192 high-speed differential pairs are supported.

### First Products to Blend VPX and ASI

One of the first products on the market based on ASI and the VPX format is the VPX6-185 from Curtiss-Wright Controls Embedded Computing. The 6U VPX6-185 delivers a nominal backplane bandwidth of 8 Gbytes/s via its four ASI, and includes the processing power of Freescale's 8641 single/dual-core PowerPC processor, two PCI Express VITA 42 XMC/PMC sites and an extensive list of standard features such as three Gigabit Ethernet (GbE) interfaces, serial ports and mass storage interface options.

The VPX6-185's processing engine is the Freescale 8641 single/dual-core PowerPC device. With its dual integrated 64-bit memory controllers, the 8641 offers vastly increased memory performance compared to prior generations of PowerPC processors, translating directly to reduced execution times for user application software. For numeric-intense processing, the 8641 offers the powerful AltiVec instruction set extension, which

performs up to 8 floating-point operations per cycle. For a dual-core device operating at 1.5 GHz this results in 24 Gflops of peak floating-point performance.

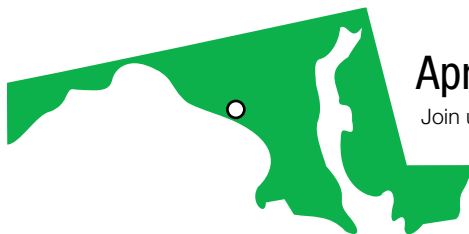
The native capabilities of ASI and the option for PCIe interoperability make ASI a compelling fabric choice for mil/aero embedded computing, where one often finds a combination of multiple cooperating processor cards tackling sensor data processing and mission-management applications along with a range of I/O boards for system interfacing and control. ASI together with the VPX module format provide a quantum leap in backplane data transfer capabilities. ■■

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# Main Feature

Switched Fabrics: Military Update

## Switched Fabric Schemes Enable Right-Sizing to an Application

Fabric schemes like VXS and VSP make it easier for military system developers to match the structure of the problem to the interconnect topology used.

Bob Walsh, Field Applications Engineer  
Tek Microsystems

One are the days when it was necessary to “shoehorn” a problem into the available solution. As embedded multicomputer signal processing systems have evolved, it’s now possible to let the solution mirror the problem to be solved. In the past, the alternatives were to solve problems first with bus-oriented systems, and later with parallel switched architectures. Now the advent of serial switched fabrics allows the design of systems that more closely model the problem to be solved. VITA 41 (VXS) and VITA 55 (Virtual Streaming Protocol) are the latest stages in this evolution. VXS and VSP allow processing and interconnection to be combined in ways that were not possible in the past.

In addition to standard topologies such as stars and dual stars, VXS allows much more interesting topologies, such as rings, meshes and partial meshes. These topologies allow the designer to match the structure of the problem to achieve a much more efficient and effective design. Now better solutions can be designed using the advanced approach made possible by VITA 41 and VITA 55.



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Figure 1

The next-generation E-2D Advanced Hawkeye aircraft will be the U.S. Navy's next-generation airborne early warning and battle management system. The E-2D Advanced Hawkeye will be the latest version of the Hawkeye family of aircraft and will feature a new radar system along with other advanced capabilities. Shown here is the E-2D's predecessor, the Hawkeye E2-C.

### Common Signal Processing Applications

Embedded multicomputer signal processing systems are used to solve a variety of problems. One of the most common is multichannel signal acqui-

sition and analysis. These systems do things like signal analysis, beam forming or jammer suppression. They typically have many input data channels that are processed and combined into relatively few output channels. The

# Design to Deployment with One Graphical Environment

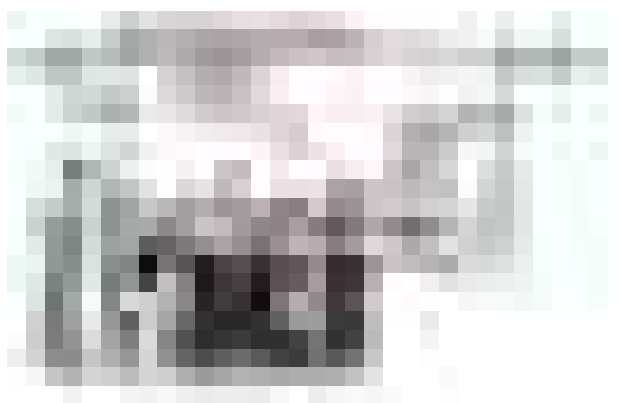


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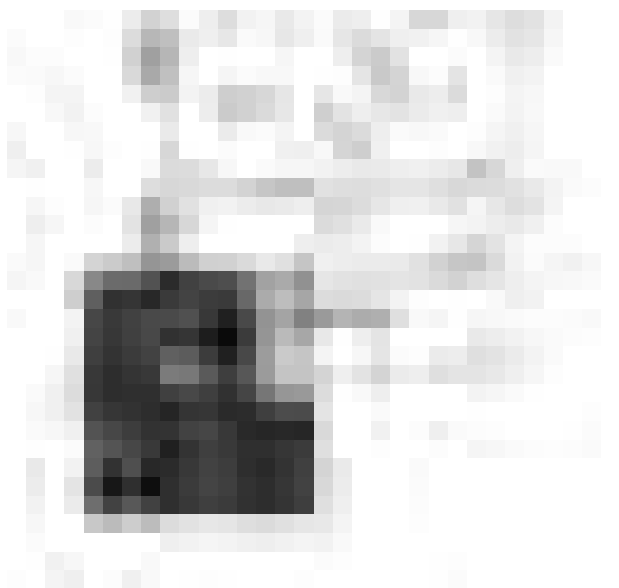
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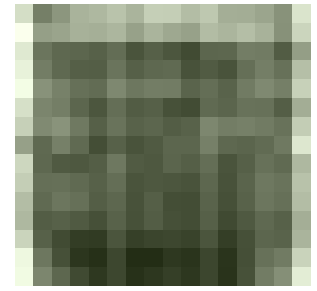
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APIC (add'l PCI interrupts)	9	9	9		9	9	9	9	9	9	9	9	9	9	9	9	9
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ACPI Power Mgmt	2.0	2.0	2.0		1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	256	256	256	32	32
Max Onboard DRAM (MB)	512	512	512		512	512	512	512	512	512	512	512	✓	✓	✓	✓	✓
RTD Enhanced Flash BIOS	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Nonvolatile Configuration	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Quick Boot Option Installed	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Fail Safe Boot ROM	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
USB Boot	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Watchdog Timer & RTC	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
IDE and Floppy Controllers	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSD Sockets, 32 DIP	1	1	1		1	1	1	1	1	1	1	1	1	1	1	2	1
Audio	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
TFT Panel TTL or LVDS	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SVGA Interface	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
AT Keyboard/Utility Port	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PS/2 Mouse	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
USB Mouse/Keyboard	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RS-232/422/485 Ports	2	2	2		2	2	2	2	2	2	2	2	2	2	2	2	2
USB 2.0 Ports	2	2	2		2	2	2	2	2	2	2	2	2	2	2	2	2
USB Ports	1	1	1		1	1	1	1	1	1	1	1	1	1	1	1	1
10/100Base-T Ethernet	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
ECP Parallel Port	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
aDIO™ (Advanced Digital I/O)	18	18	18		18	18	18	18	18	18	18	18	18	18	27	18	18
multiPort™ (aDIO, ECP, FDC)	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
ROM-DOS Installed	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DOS, Windows, Linux	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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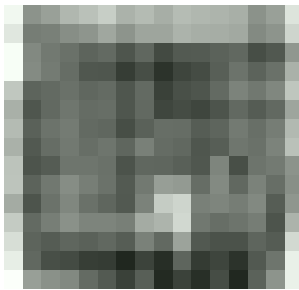
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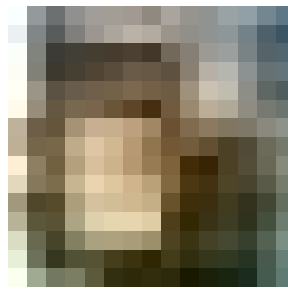
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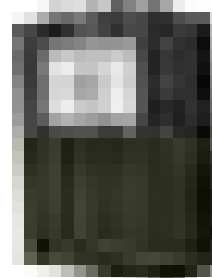
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		SDM6440HR	SDM6540HR	SDM7540HR	SDM8540HR	DM6420HR	DM6430HR	DM7520HR	DM7530HR	DM6620HR	DM6812HR	DM6856HR	DM6888HR	DM6956HR	DM7820HR
Bus	AT Expansion Bus	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master			✓	✓			✓	✓						✓
	McBSP™ Serial Ports		✓	✓	✓			✓	✓						
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16	16						
	Differential Inputs	8	8	8	8	8	8	8	8						
	Max Throughput (kHz)	500	1250	1250	1250	500	100	1250	100						
	Max Resolution (bits)	12	12	12	12	12	16	12	16						
	Input Ranges/Gains	3/4	3/7	3/7	3/7	3/4	1/4	3/6	1/4						
	Autonomous SmartCal™	✓	✓	✓	✓										
	Data Marker Inputs	3	3	3	3	3		3							
Conversions	Channel-Gain Table	8k	8k	8k	8k	8k	8k	8k	8k						
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓	✓						
	A/D FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						
	Sample Counter	✓	✓	✓	✓	✓	✓	✓	✓						
	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓	✓	✓					✓
	SyncBus		✓	✓	✓			✓	✓						
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	16	16	48	32	64	32	48
	Bit Programmable I/O	8	8	8	8	8	8	8	8	8	24				48
	Advanced Interrupts	2	2	2	2	2	2	2	2	2	2				2
	Input FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						2M
	Opto-Isolated Inputs											16	48	16	
	Opto-Isolated Outputs											16	16		
	User Timer/Counters	2	3	3	3	2	2	3	2	3	3				10
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓
	Relay Outputs													16	
Analog Out	Analog Outputs	2	2	2	2	2	2	2	2	4					
	Max Throughput (kHz)	200	200	200	200	200	100	200	100	200					
	Resolution (bits)	12	12	12	12	12	16	12	16	12					
	Output Ranges	4	4	4	4	3	1	4	1	4					
	D/A FIFO Buffer		8k	8k	8k			8k		8k					

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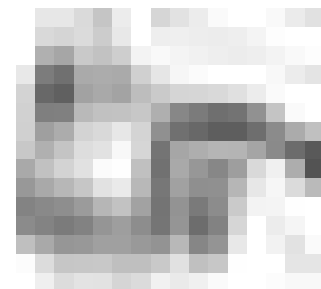
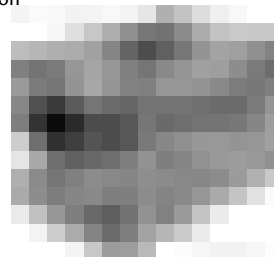
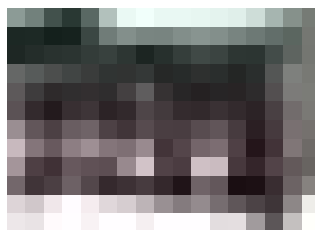
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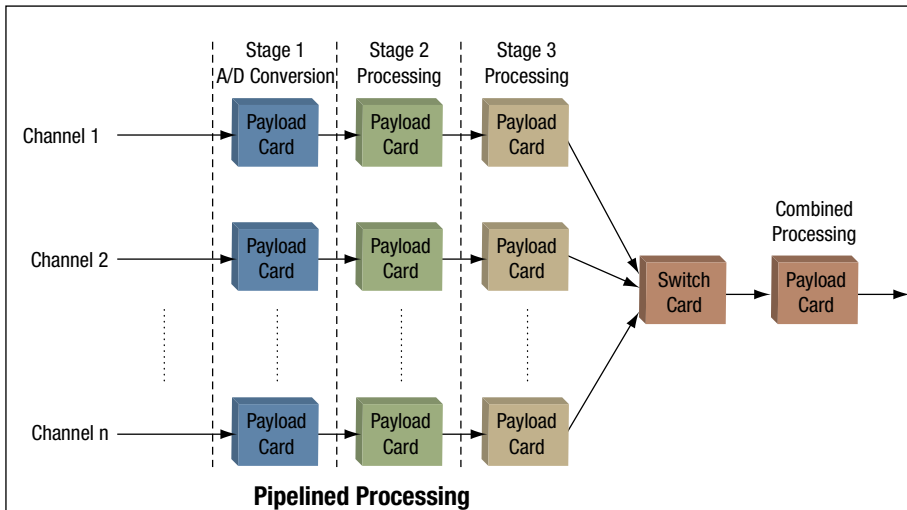
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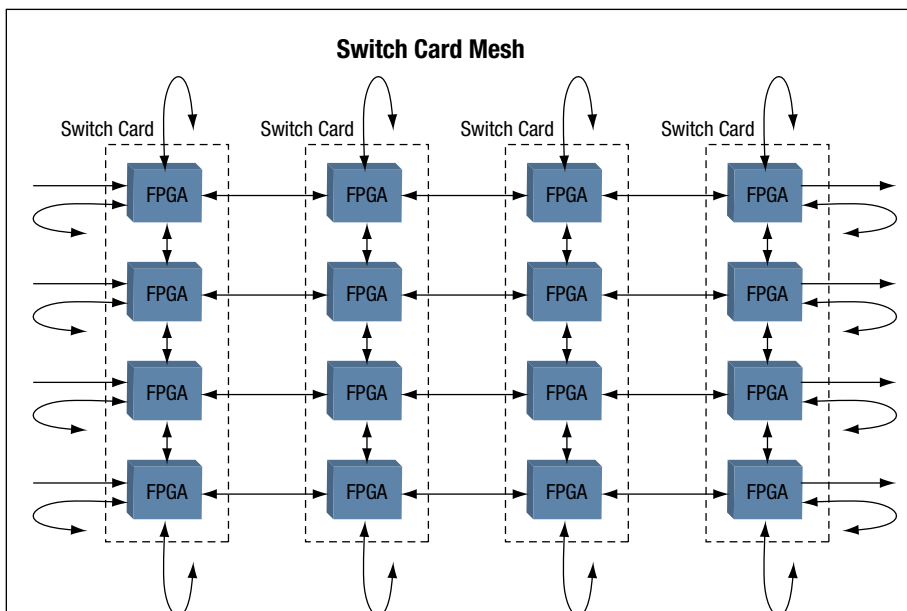
**Figure 2**

Using the VXS standard, a backplane could be laid out that simply interconnected payload cards in some sort of ring, mesh, or partial mesh, or a dataflow chain. The input signals could come to a set of A/D cards, which then use the backplane to transfer the digitized signal to a processor card, or perhaps a chain of processing cards. Several signals could be processed by parallel chains in this manner, and the last stages could be connected through a switch card to a final stage that combined the signals together for final processing.

inputs usually run in continuous streams, with no interruptions between blocks or frames.

Another common application is synthetic aperture radar (SAR). An example along those lines is the next-generation E-2D Advanced Hawkeye aircraft, which will feature a new radar system (Figure 1). Embedded SAR processors do 1D FFTs on the rows of a matrix, then the processors exchange data with the other processors in a “corner turn” operation, and finally the processors do another 1D FFT. Accomplishing the corner turn across a large number of processors is often the limiting factor on the system performance, since each processor has to exchange data with all the other processors.

Embedded multicomputer systems are also used to do conventional image processing, things like image enhancement or target recognition. Each processor processes a sub-image, and then exchanges data with its nearest neighbors. Designing these systems can be problematic, especially when dealing with the edges of the image. The most straightforward approach models the solution as a grid, or mesh of processing nodes.



**Figure 3**

Shown here is a system with a backplane that routes the switch card I/O channels so that the individual FPGAs are connected in a fully connected mesh. Such a scheme would be an immensely powerful system for problems such as image processing.

## Legacy Approaches

The first embedded multicomputer systems were based on shared memory architectures, or bus architectures such as VMEbus. In these systems there was one path available for the processing nodes to communicate, or to move data in or out of the system. If one transfer was in progress, everything else had to wait. Besides being relatively slow, this required the designer to pay careful attention to the order in which transfers occurred, and to make sure that high priority transfers were not impeded by lower priority exchanges. Solving any signal processing problem on one of these systems was definitely a chore.

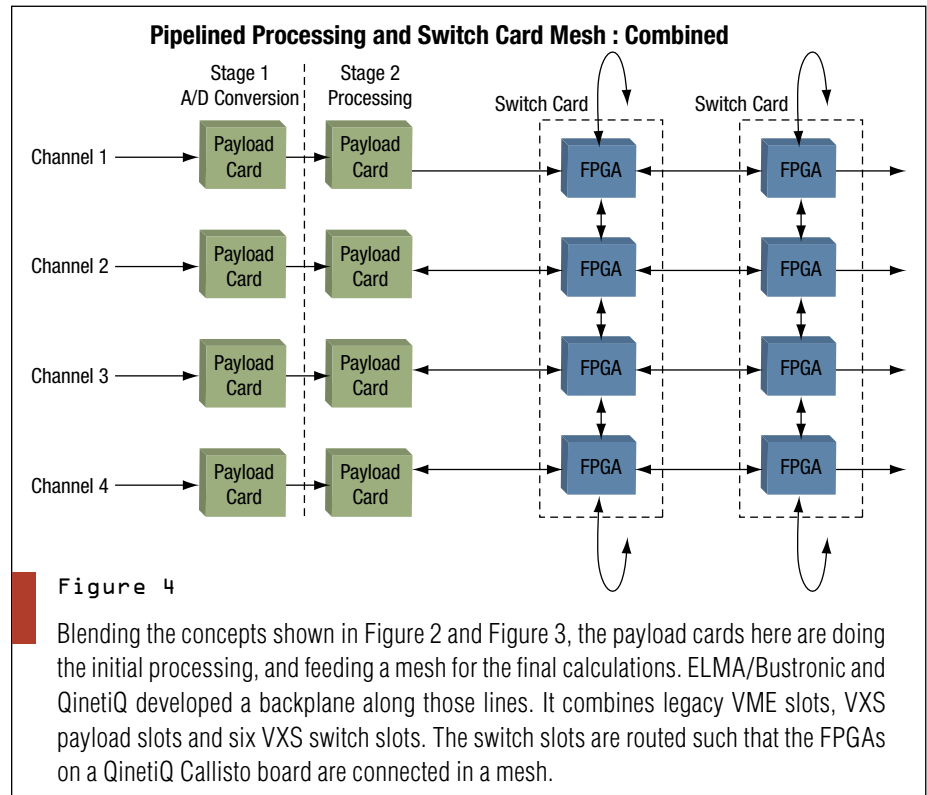
Parallel fabrics, such as Mercury Computer's RACEway, added raw speed and the ability to have multiple transfers going on at the same time. This allowed much higher performance than standard VMEbus systems. RACEway uses switch ASICs that are either on the individual cards, or on overlays that are fitted over the backplane connectors. The individual

switches are limited to six or eight ports each, but they can be stacked in hierarchies that allow large numbers of nodes to be connected to the fabric.

That's a vast improvement over a simple bus, but it still has some limitations. The first level switches are fully connected, but there are limited paths between the first level and higher levels. This means that transfers have to take place in a specific order to avoid conflicts. Continuous data streams must be buffered somehow to avoid overflows caused when crossbar paths conflict. Design approaches such as rings or meshes can be difficult to implement.

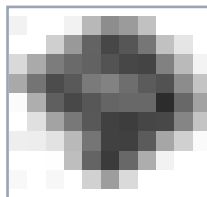
### Basics of VXS

VITA 41/VXS brings some new tools to the party. VXS cards come in two flavors: payload cards and switch cards. Payload cards are essentially 6U VME cards with enhanced P0 connectors. Switch cards use special high-speed connectors to provide interconnects between multiple



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payload cards. The payload cards support up to 2.5 Gbytes/s of bandwidth, which is an order of magnitude faster than previous generations. Each switch card supports up to 18 payload cards.

The VITA 41 standard defines a layered architecture. The base specification describes the mechanical, connector, power and system management interfaces, but it does not define a specific

switched fabric interconnect. Each possible switch fabric is defined in a protocol standard that maps the switched fabric protocol into the high-speed differential pair connections laid out in VITA 41.0. There are VITA 41 protocol standards defined for InfiniBand, Serial RapidIO, Gigabit Ethernet, PCI Express and Advanced Switching.

## VXS Solutions

The VXS base standard describes one specific example of a VXS system using a combination of payload and switch cards to implement a dual-star fabric topology. Each payload card has a 1.25 Gbyte/s connection to each of the two switch cards. This is conceptually not much different than the previous generation parallel switched architectures, but there are important advantages. The interconnection paths run much faster than RACEway, for instance, and each payload card has two paths to switches instead of just one.

If the switch is designed to be flat instead of hierarchical, then it would not be necessary to be as careful about the order that transactions take place, since there would be fewer contending paths. This topology would make a SAR corner turn faster and easier to accomplish. The faster interconnection paths would allow faster processing rates than previous generations, and it would be easy to scale the system to handle more rows and columns by adding payload/processing nodes.

The VXS standard allows more than simple star topologies. It does not mandate any specific topology—the designer can use the one that best solves the problem. In fact, there is no requirement that a switch card be in the system at all. A backplane could be laid out that simply inter-connected payload cards in some sort of ring, mesh, or partial mesh, or a dataflow chain. The input signals could come to a set of A/D cards, which then use the backplane to transfer the digitized signal to a processor card, or perhaps a chain of processing cards. Several signals could be processed by parallel chains in this manner, and the last stages could be connected through a switch card to a final stage that combined the signals together for final processing. This could be used to build a beam former, or an anti-jamming system. This idea is illustrated in Figure 2.

In fact, the concept of a switch card does not actually require that the card perform a switch function. In the example above, it would make more sense to build a card with the switch card I/O connections, but to put the processing hardware on that card. QinetiQ's Callisto Board is

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## Main Feature

just such a board. It has five Xilinx Virtex-II Pro FPGAs on a VXS switch card. The FPGAs can be programmed with a fabric protocol core, or the signal processing core, or perhaps both, if that is appropriate. To carry this just a bit farther, a backplane could be developed that routed the switch card I/O channels so that the individual FPGAs were connected in a fully connected mesh.

This would be an immensely powerful system for problems such as image processing. An example of this is shown in Figure 3. A more complete system is shown in Figure 4, with payload cards doing the initial processing, and feeding a mesh for the final calculations. A real example of this has been developed in collaboration with ELMA/Bustronic and QinetiQ. This backplane combines legacy VME slots, VXS payload slots and six VXS switch slots. The switch slots are routed such that the FPGAs on a Callisto board are connected in a mesh, like the one shown in Figure 4.

### Switched Fabric vs. Point-to-Point Interconnection

In several of the above examples, there is really no point in implementing a switch fabric for connections that are really just point to point. While FPGAs can implement the fabric protocol on each end, the resources are better used for signal processing functions. Tekmicro and QinetiQ have recently co-sponsored a new standard called Virtual Streaming Protocol (VSP), also designated VITA 55. VSP implements a low overhead point-to-point link between FPGA-based endpoints and can be used on a variety of physical layers.

One implementation is being defined as VITA 41.5 and provides point-to-point interconnect between VXS payload and switch cards using Xilinx's Aurora low-level protocol. Another implementation will be defined to support parallel bus links between FPGA devices on a board. The range of physical implementations will allow the VSP protocol to be utilized

throughout a FPGA processing cluster, providing a common method of interconnect for the user whether the interface is to an adjacent FPGA on the same card or to an FPGA on another switch card or even in another chassis.

### Mapping to Next-Gen Processing Needs

Solutions that map the problem to be solved onto the solution architecture result in designs that are higher performing, more flexible and more efficient than before. VITA 41/VXS and VITA 55 allow an important step forward in building systems that mimic the structure of important problems that are typically faced by embedded signal and image processing systems. ■■

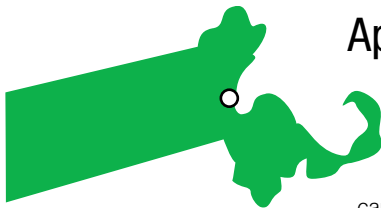
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## Obsolescence Management Now Includes “Getting the Lead Out”

Now that military engineers must deal with the effects of RoHS compliance on top of other component obsolescence problems, the DoD and its suppliers are developing several programs to help.

Ann R. Thryft  
Senior Editor

**A**growing infrastructure of companies and organizations are available to help military system designers cope with component obsolescence, often referred to as Diminishing Manufacturing Sources and Materials Shortages (DMSMS). *COTS Journal's* “Seventh Annual End-of-Life Supplier Directory,” following this article, lists over 30 of those players and what they do.

As the EOL Directory shows, there are a number of ways to deal with the problem of a chip that's gone end-of-life. Numerous after-market chip suppliers stock inventories of obsoleted devices. Among them is a mix of small firms specializing in after-market business, as well as large distributors who include after-market products in their portfolio. In addition, some packaging firms perform custom assembly of obsolete ICs using existing wafers and die.

The Directory includes both key DoD organizations and commercial firms involved in the problems of component obsolescence, as well as the services

provided by each. The three DoD organizations are the Defense Microelectronics Activity (DMEA), the Defense Supply Center Columbus (DSCC) and the Government-Industry Data Exchange Program (GIDEP).

### Lead-Free: A Global Transition

However, there's a major new wrinkle to the management of obsolete parts. An additional set of concerns has been added to complicate the issue, as the deadline looms for compliance

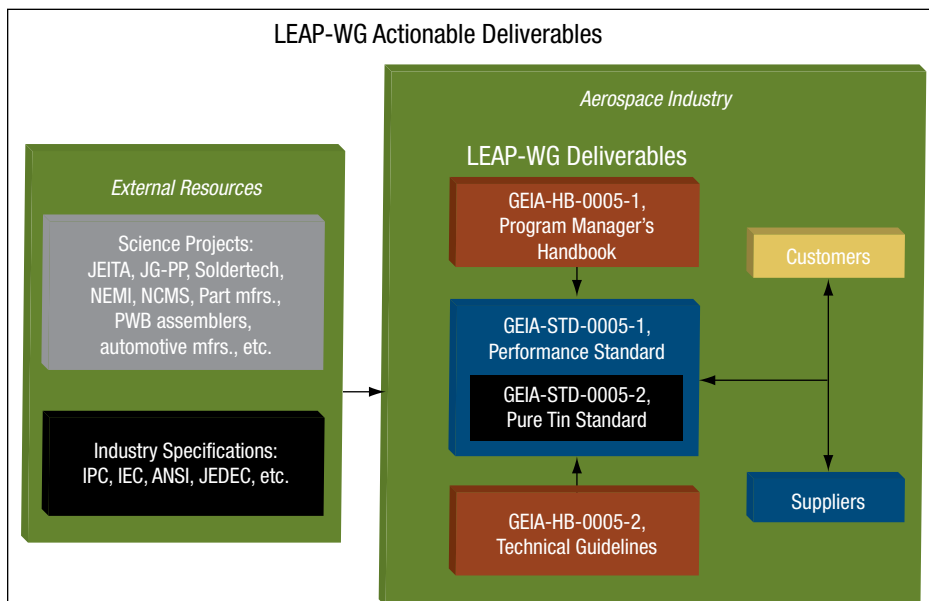


Figure 1

Source: Lloyd Condra, Boeing

Three out of the four documents to be produced by the Lead-Free Electronics in Aerospace Project Working Group (LEAP-WG) are in the last stages of the Government Electronics and Information Technology Association (GEIA)'s approval process. A fourth, the GEIA-HB-005-2, Technical Guidelines, is still in progress. LEAP-WG was formed to develop and implement actionable deliverable items in the form of best practices and technical guidelines, by involving members from all stakeholders.



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with the European Restriction of Hazardous Substances (RoHS) directive. It restricts not only lead, but also cadmium, mercury, hexavalent chromium, polybrominated biphenyl and polybrominated diphenyl ether. Although military equipment is technically exempt from this and similar initiatives, that status could easily change. Meanwhile, related legislation is underway in Japan and China.

Even if military equipment does remain exempt programs will be affected, since commercial component manufacturers and board makers supply both the military electronics market and the much larger, worldwide commercial electronics market.

As far as the DoD is concerned, the transition to lead-free electronics is a global one, according to Kevin Rankin, chief of the DMEA's Microelectronics Systems Branch. "Lead-free brings new and re-emerging failure modes in elec-

tronics" he says. "Lead-free exemptions will only buy us a little time. Programs are needed to develop and implement a lead-free transition strategy."

In most cases, component manufacturers have not found it cost-effective to produce both lead-free and leaded components. "A good number are phasing out their lead-containing components, since their main market is not military/aerospace," says Vance Anderson, a DMEA program manager focused on special projects, including RoHS.

For defense and aerospace systems, this poses special problems, since they have several unique requirements, such as high reliability, a very long service life and extended temperature ranges. The primary impacts on military/aerospace systems are performance problems with lead-free solder materials, failures caused by tin "whiskers," the availability of leaded solder and components, and the need for new

processes and configuration control to track which repairs used leaded or lead-free solder. Strategies for commercial solutions to the lead-free transition are therefore not necessarily suitable to military/aerospace applications, says Anderson.

Several different military/aerospace lead-free efforts are underway. The University of Maryland's Computer Aided Life Cycle Engineering (CALCE) Electronic Products and Systems Center (EPSC) has produced a number of projects and tools related to lead-free issues and the tin whisker problem. It also possesses considerable research and survey data on the status of manufacturers transitioning to lead-free parts.

In other efforts, NASA's Goddard Space Flight Center has conducted research efforts on tin whisker effects. So has the Navy's Office of Naval Research, in conjunction with CALCE, NASA and several aircraft manufacturers and their suppliers.



The Joint Council on Aging Aircraft/Joint Group on Pollution Prevention and NASA Kennedy perform lead-free solder testing for high-reliability applications.

### The LEAP-WG: Best Practices, Technical Guidelines

In 2004, the Lead-Free Aerospace Electronics Working Group was formed by the Aerospace Industries Association

(AIA). Now called the Lead-Free Electronics in Aerospace Project Working Group (LEAP-WG), its purpose is to develop and implement actionable deliverable items in the form of best practices and technical guidelines that enable the aerospace industry and the military to accommodate the global transition to lead-free electronics.

Under the joint aegis of the AIA, the Avionics Maintenance Conference (AMC)

and the Government Electronics and Information Technology Association (GEIA), the LEAP-WG includes members from all stakeholders in different market segments, geographic regions and parts of the supply chain. "The goal was to tie in all of the parties who were forced to address the lead-free issue in the military and the aerospace/high-reliability industry," says Anderson.

The LEAP-WG's actionable deliverables consists of four documents. The first is GEIA-HB-0005-1, the Program Manager's Handbook. This will be used to address all issues related to lead-free electronics, such as logistics, warranty, design, production, contracts and procurement. The second is GEIA-STD-0005-1, Performance Standard for Aerospace Electronic Systems Containing Lead-Free Solder. Aerospace electronic system customers will use this document to communicate requirements to aerospace electronic system suppliers.

The third document, GEIA-STD-0005-2, is the Technical Guidelines for Mitigating the Deleterious Effects of Pure Tin in Aerospace Electronic Systems. Finally, GEIA-HB-0005-2 is the Technical Guidelines for Using Lead-Free Solder in Aerospace Applications. Suppliers will use these guidelines to select and employ lead-free solder alloys, as well as other materials and processes.

While the LEAP-WG was formed to generate documentation, the DoD's Executive Lead-Free Integrated Product Team (ELFIPT) looks specifically at how to deal with lead-free issues within the DoD, says Rankin. A management-level group, its DoD members include representatives from the DMEA, each military service, the Defense Logistics Agency and the Federal Aviation Administration. Other members are representatives from weapon system prime contractors. A DoD Lead-Free WG has been formed that will draw from both the LEAP-WG and the ELFIPT to recommend lead-free policy and technology investment. ■■

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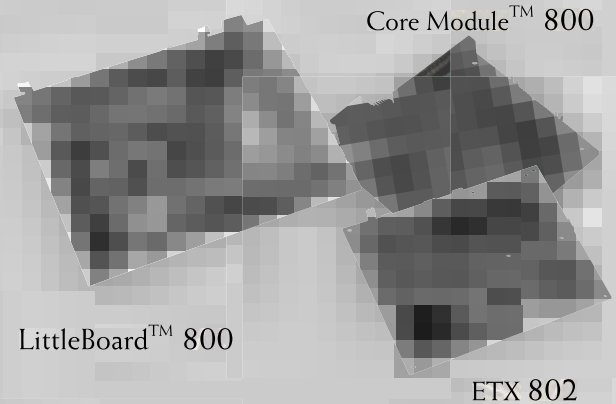
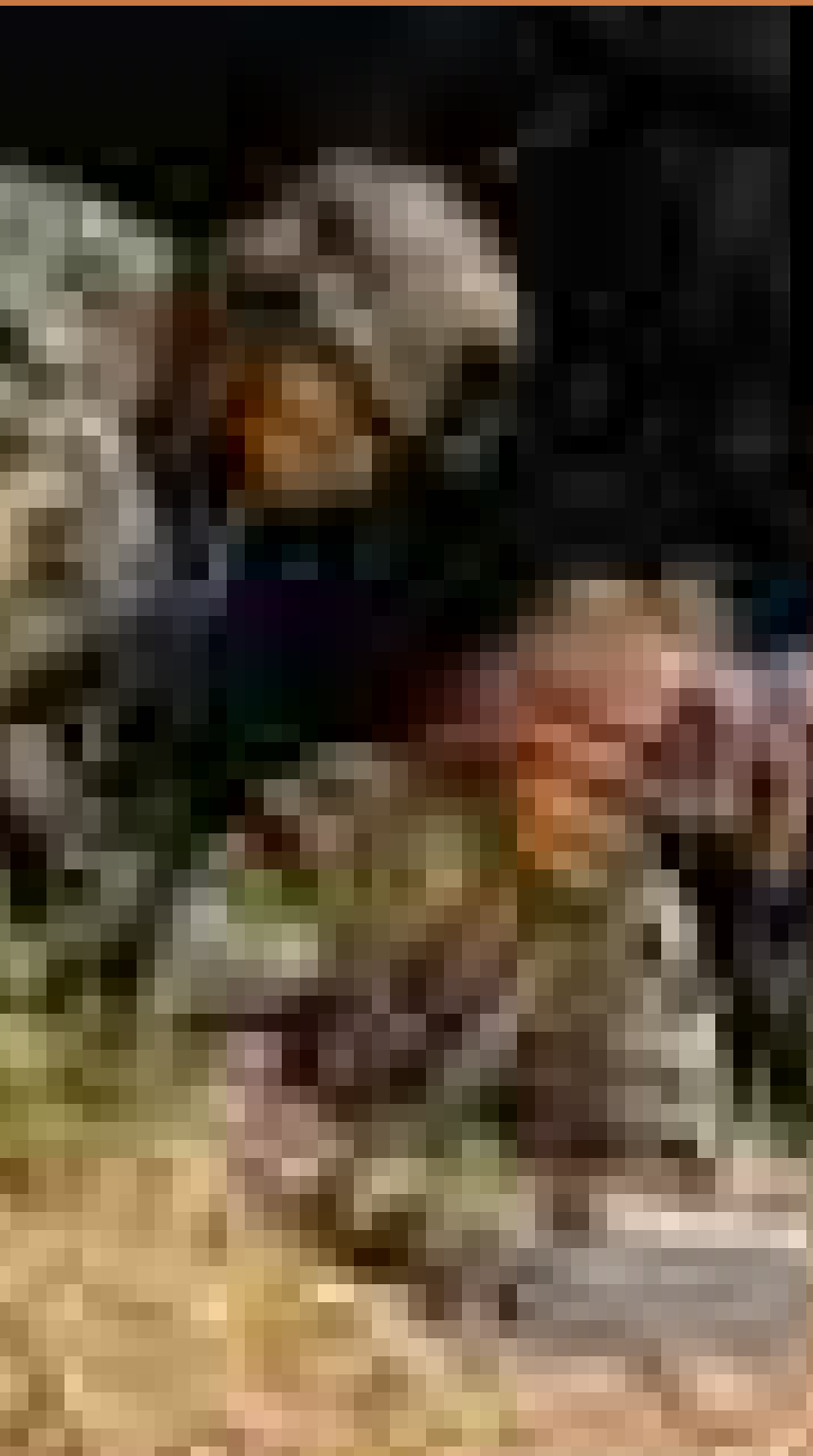
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# System Development & Test

Annual EOL Directory

Seventh Annual Directory of End-of-Life Suppliers

Company/Org.	Contact	Category	Comment
ARINC	Annapolis, MD. (410) 266-4535. [www.arinc.com].	DB, L, R	ARINC's Team implements processes to minimize the impact of obsolescence for COTS systems. ARINC identifies problems, researches solutions, determines spares shortages, performs economic life cycle cost studies to determine the right time to implement technology refreshes and provides engineering services such as reverse engineering and systems integration.
Arrow/Zeus Electronics	Purchase, NY. (914) 701-7400. [www.arrow.com].	O	Distributor targeting North America's military and aerospace markets. Focuses on high-reliability semiconductor, passives and system products.
Austin Semiconductor	Austin, TX. (512) 339-1188. [www.austinsemiconductor.com].	D, E, L, O, P, S	Deals in semiconductor components (memory, logic, linear and analog) modules and subassemblies, both standard and custom in a variety of hermetic/ceramic and plastic packages. Certifications for MIL-PRF-38535 (Class Q) and MIL-PRF-38534 (Class H). Has capabilities for Class S (space level) and radiation-tolerant manufacturing, including MIL-PRF-38534 Class 'V' Assembly. All MIL-STD-883C Methods & Conditions Service provider to the Mil & HI-REL/Space marketplace.
Avnet	Phoenix, AZ. (800) 423-4688. [www.avnet.com].	DB, E, L, O, P, R, S	Global electronics distributor with numerous value-add services from testing and screening to assembly.
CALCE Electronic Products and Systems Center	College Park, MD. (301) 405-5323. [www.calce.umd.edu].	B, DB, R, S	Widely regarded as the industry's most knowledgeable source for evaluating and using components outside of OEM specifications. Also known for expertise in design refresh planning and other DMSM management activities, parts management and supply chain assessment for quality and reliability.
Chip Supply	Orlando, FL. (407) 298-7100. [www.chipsupply.com].	D, P	Offers semiconductor die and packaging solutions. Capabilities include post wafer fab processing, including dicing, inspection, engineering and test services; obsolescence management/life cycle planning; and specialized packaging solutions, including ceramic, CSP, TAB and QML.
CPU Technology	Pleasanton, CA. (925) 224-9920. [www.cputech.com].	B, E	Uses advanced design tools in developing system-on-a-chip-based technology to produce modernized, backward-compatible embedded computing solutions and high-performance, general-purpose multi-core processors for use in military and commercial environments.
DMEA	McClellan Park, CA. (916) 231-1506. [www.dmea.osd.mil].	B, E, F, G, P	DMEA provides long-term, strategic support for the entire range of DoD systems that utilize microelectronics. DMEA uses a unique, innovative methodology to reverse-engineer microelectronic devices to determine their function and a specification; analyze possible solutions; and design, build, and test the best solution. An on-site reconfigurable foundry produces die in several critical process technologies.
DPA Components International	Simi Valley, CA. (805) 581-9200. [www.dpaci.com]. [www.dpems.com].	D, P, S	Specialty recovery process to remove and reuse die from OEM plastic or ceramic packaged parts, repackaging, upscreening and testing. Comes close to DMEA definition of "reclamation," but at a die level.
DSCC-VQ	Columbus, OH. (614) 692-0662. [www.dscclia.mil/offices/sourcing_and_qualification/].	DB, G, R	QML/QPL product for OEM procurement and logistics support to military services. Provides oversight of electronic component manufacturers for the military services.
Electronic Material Industries	Toluca Lake, CA. (818) 763-9584. [www.militarycomponents.com].	O	Buys, sells and stocks military and commercial electronic components.
Falcon Electronics	Commack, NY. (631) 351-8515. [www.falconelec.com].	L, O, S	Distributor to the avionics, military and space industry. Segregated product handling per JEDEC and MIL-STD. Offers DMS support services such as Global Semi Search and access to an extensive obsolete inventory. Also offers upscreening.

Company/Org.	Contact	Category	Comment
GD California	Livermore, CA. (925) 456-9900. [www.gdca.com].	B, O	Specializes exclusively in legacy board- and system-level products.
GIDEP	Corona, CA. (951) 898-3213. [www.gidep.org].	DB, G, R	The DoD's centralized database for DMSMS issues; hotlinks to numerous industry references on DMSMS. Host for the DoD DMSMS Knowledge Sharing Portal (DKSP).
IEC/IECQ	Geneva, Switzerland. +41 22 919 02 11. [www.iecq.org].	R	IEC generates international standards for the practice of uprating components and using them in systems. IECQ conducts the IEC's certification program for electronic components, processes and related materials, including aerospace.
IHS	Englewood, CO. (303) 397-2896. [www.IHS.com].	DB, L	4DOnline Parts Universe catalogs more than 14 million electronic parts from over 500 manufacturers in 350+ categories. HAYSTACK contains over 100 million parts in Federal Supply Catalog and over 40 U.S. Army, Navy, Air Force and related databases. Fasteners eCatalog enables identification, specification and sourcing of aerospace and defense standard fasteners/hardware.
innovASIC	Albuquerque, NM. (505) 883-5263. [www.innovasic.com].	E	A fabless semiconductor company that specializes in producing replacement ICs. It clones ICs as replacements for chips discontinued by the original manufacturer.
Inventory Locator Service (ILS)	Memphis, TN. (901) 794-5000. [www.ilsmart.com].	DB, L	Focuses primarily at the subsystem level.
L-3 Communications, Advanced Products & Design	San Diego, CA. (858) 527-6100. [www.L-3Com.com/apd].	B, E, P	Rapid Retargeting engineering services developer/provider for board-level electronic components and subsystems. Approach relies on reconfiguring hardware and software to be form, fit and functional replacements.
Lansdale Semiconductor	Tempe, AZ. (602) 438-0123. [www.lansdale.com].	D, E, O, P	Aftermarket support of over 3,000 obsolete ICs from Motorola, Philips, Intel, National, AMD and others. Manufactures products using the original tooling to ensure same performance and quality. QML certified to MIL-PRF-38535.
Maxwell Technologies	San Diego, CA. (858) 503-3300. [www.maxwell.com].	E, P	Uses MCM package as form, fit and functional replacement. Company's Rad-Pak technology enables commercial devices to meet space requirements. Fabless, QML-certified, with radiation testing and laboratory analysis capabilities.
Minco Technology Labs	Austin, TX. (512) 834-2022. [www.mincotech.com].	D, O, P	Semiconductor, processor and tester serving military, space and commercial industries.
MTI	Fort Walton Beach, FL. (850) 664-6070. [www.mtifwb.com].	B, DB, E, L, R	Obsolescence management software, engineering services, design, redesign and manufacturing.
NAPCO International	Hopkins, MN. (952) 931-2400. [www.napcointl.com]	B, DB, D, O, P, S	A global engineering, materials management, procurement, packaging, containerization and light manufacturing company specializing in the support of military tracked and wheeled equipment.
Now Electronics, N2O Semi Division	Huntington, NY. (800) 669-3532. [www.n2osemi.com].	L, O, P	Distributor specializing in all types of obsolete memory and specialty semiconductors. Provides support for legacy products from Dens-Pak, as well as support for DMS for White/EDI, IDT, Cypress, MOSAIC, APTA/HMP and Austin. Mil-Spec and other advanced packing and testing services available.
Pikes Peak Test Labs	Colorado Springs, CO. (719) 596-0802. [www.pptli.com].	E, L, O, P, S	Lab experienced in electronic component testing and evaluation, including environmental testing, destructive physical analysis, failure analysis. Does high- and low-temperature testing and upgrade screening for commercial, industrial and military parts.
Precience	Silver Spring, MD. (301) 421-9054 [www.precience.com].	DB	Assists in up-front component selection, lifecycle prediction algorithm, EOL notification.

## System Development & Test

Company/Org.	Contact	Category	Comment
QP Semiconductor	Santa Clara, CA. (408) 737-0992. [www.qpsemi.com].	DB, D, E, F, R	QML manufacturer and supplier of high-reliability hermetic ICs for military, aerospace and industrial applications; solutions for DMSMS and EOL problems.
Richardson Electronics	LaFox, IL. (630) 208-2200. [www.rell.com].	DB, O, P	Distributor serving RF and wireless communications, industrial power conversion, medical imaging, security and display systems markets. Engineering services are available to aid product manufacturing, systems integration, prototype design and part logistics from design-in through after market stages.
Rochester Electronics	Newburyport, MA. (978) 462-9332. [www.rocelec.com].	D, F, O, P, R	Authorized/franchised supplier of aftermarket parts for over 40 semiconductor suppliers with over 500 million finished parts and 3 billion die. Manufactures over 15,000 aftermarket devices, from commercial to fully certified military. Offers packaging and testing to extend product life even further.
Sarnoff	Princeton, NJ. (609) 734-2168. [www.gemes.com].	E, F, R, P	Government-authorized contractor for Generalized Emulation of Microcircuits (GEM) program.
Sensitron Semiconductor	Deer Park, NY. (631) 586-7600. [www.sensitron.com].	B, D, E, F, P, R, S	Full-service provider including R&D, design, wafer fabrication, packaging, screening, testing and engineering. Maintains a wafer fabrication clean room and a microelectronics manufacturing clean room.
Sypris Test and Measurement	Orlando FL. (800) 839-4959. [www.wetest.com].	S	Offers test and calibration services to space and defense prime contractors, government agencies, and commercial manufacturers, including automotive, avionics, telecom and medical. Services include semiconductor and passive component test, wafer probe, product test and evaluation, and repair and calibration of general electrical and mechanical test equipment. Fixed locations, on-site locations and mobile calibration facilities nationwide. ISO-9001:2000 registered, DSCC-approved, A2LA (ISO/IEC-17025) accredited and ISTA-certified.
T.S.I. Microelectronics	Danvers, MA. (978) 774-8722. [www.tsimicro.com].	D, E, O, P	Manufactures custom thick and thin film hybrids to SCDs for DSCC and military OEMs. Offers custom IC packaging into hermetic packages. Design and reverse engineering; second source to various obsolete hybrid circuits and discrete semiconductors.
Total Parts Plus	Fort Walton Beach, FL. (850) 244-7293. [www.totalpartsplus.com].	DB	Internet obsolescence and material content databases for all grades of semiconductors as well as database enhancement services.

Abbreviation	Categories	Explanation
B	Board level	Solves board-level DMS problems (as opposed to component-level problems).
DB	Database	Provides a database covering topics such as alternate sources, devices that are obsolete, cross-references or uprating results.
D	Die processor	Refers to processing OEM die, not an emulated solution.
E	Emulation/reverse engineering	Vendor may emulate a DMS device in a gate array or full-custom device, or provide a pseudo-form, fit and functional equivalent.
F	Foundry	Has foundry capability to fabricate wafers
G	Government agency	—
L	Locator	The vendor provides a service to locate DMS components and boards/systems.
O	Obsolete inventory	Maintains OEM inventory in die or packaged form.
P	Specialty packaging	Packages components as monolithic or multi-chip modules.
R	Industry reference	Denotes an organization or company with widely recognized knowledge or information concerning the DMS industry.
S	Uprating/upscreening	Performs uprating or upscreening.



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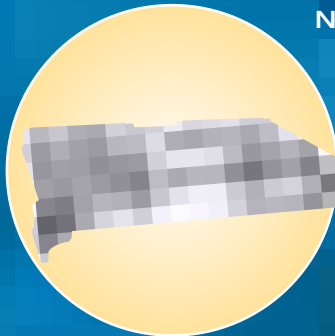
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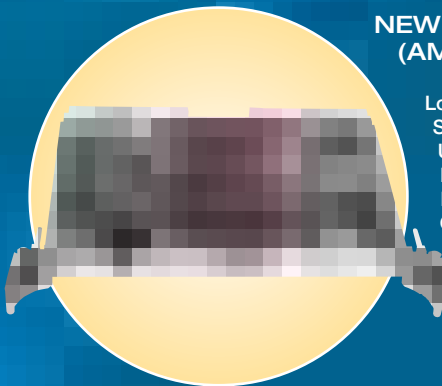
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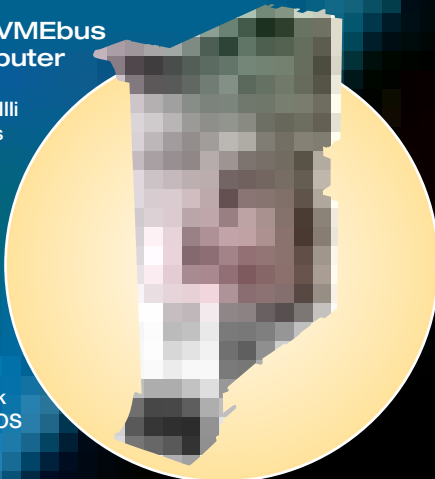


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# Technology Focus

Processor PMCs

## Processor PMCs Boost Performance, Flexibility in Mil Apps

Increasingly sophisticated systems are based on PMC, the military's mezzanine card of choice. The processor PMC enables highly integrated defense applications that demand high performance, lots of I/O throughput and low power consumption.

Ann R. Thryft  
Senior Editor

**P**rocessor PMC technology has flourished in military applications for several years now, even before the VITA Standards Organization (VSO) defined the PrPMC format in VITA 32. Since then, the follow-on standards VITA 39, which defines PCI-X on both PMC and PrPMC, and VITA 42, the base mechanical spec for support of high-speed switch fabric interconnects, have broadened its use in defense systems.

Today's military system designs incorporate PrPMC cards for a wide range of functions. What's the appeal? The PrPMC concept turns the idea of a mezzanine board inside out. While mezzanines were originally thought up to provide standard or custom I/O expansion on an SBC, the PrPMC takes out the SBC's computing core—consisting of faster-changing processors and memory—and puts it on an upgradeable module.

Meanwhile, the baseboard becomes a platform for I/O created with custom designs, or slower-changing I/O. Since it can take awhile before a system is deployed, and factoring in the need for field upgrades, the result is that military applications with longer design cycles can reap the benefits of flexibility, performance and cost control.

Processor PMCs are flexible in other ways, too. They can act as either host of the local PCI bus (monarch mode) or as a peripheral (non-monarch mode) on the local PCI bus. They are not limited to use in standard 6U VME and 6U CompactPCI applications, either. Often, they end up mounted on non-standard baseboards of different sizes and shapes.

When PrPMCs first emerged, components on most cards were limited to a processor, main memory and a PCI interface. Today, PrPMCs integrate some of the fastest CPUs available and can be used for highly specialized processing functions. High-speed system, memory and I/O interfaces, symmetric multiprocessing, dual-core high-speed CPUs, PCI-X bus interfaces and multiple ruggedization levels are some of the possibilities with current PrPMCs.

In many highly integrated defense applications such as flight computers, software defined radio, and command, control and communications systems, signal processing and control subsystems must meet the conflicting requirements of high I/O throughput and low power. Today's PrPMCs are stepping up to this task with sophisticated power management schemes and low-voltage processor options. Others offer the ability to program and reprogram a processor's speed to fine-tune the board's power consumption to the minimum required for a specific application. ■■



*Courtesy of U.S. Air Force.*

**Figure 1**

High-performance PrPMC cards provide the computing core in host and peripheral modes for a wide range of military applications, including flight computers, SIGINT and military comms. The Air Force's U-2 Dragon Lady, a high-altitude, multi-intelligence reconnaissance aircraft that can fly above 70,000 feet, provides near-real-time imagery and signals intelligence to warfighters and national authorities in support of Operation Iraqi Freedom.



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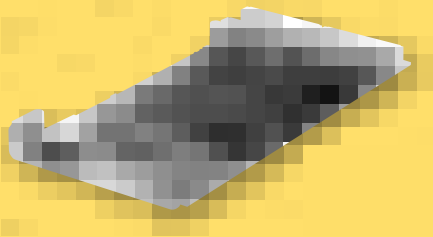
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# Technology Focus:

## Processor PMCs Roundup

### PowerQUICC III Card Provides Protocol and Packet Processing

Protocol and packet processing used to be strictly a system box-level concept. Processor PCI mezzanine cards (PrPMCs) enable developers to pack a lot more specialized processing into a smaller space. Now some PrPMCs even bring dedicated protocol and packet processing right onto the PrPMC itself. An example is Artesyn's Pm8540, a PrPMC based on the MPC8540 PowerQUICC III



communications processor. The card provides a simple way to add protocol processing and system management capability to communications systems equipped with PMC or PTMC expansion slots, including Artesyn's own Katana AdvancedTCA and PICMG 2.16 blades.

The Pm8540 features two Gigabit 10/100/1000BaseT Ethernet ports, routed to the PMC connector, and one 10/100BaseTX Ethernet port, routed to the module's front bezel. The Pm8540 features up to 512 Mbytes of SDRAM, 32 Mbytes of flash memory and an I2C bus system management controller. A four-channel DMA controller facilitates high-speed data movement between module resources. The MPC8540 processor's PowerPC e500 core delivers a peak performance of 2310 MIPS at 1 GHz. It features 256 Kbytes of L2 cache, a DDR SDRAM memory controller, two Gigabit 10/100/1000BaseT Ethernet controllers, a 10/100 Ethernet controller, a 133 MHz 64-bit PCI/PCI-X controller, a parallel RapidIO controller and the OCeAN non-blocking crossbar switch fabric.

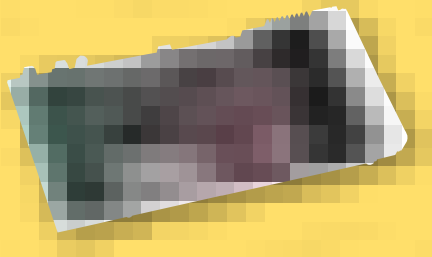
The Pm8540's mezzanine interface complies with IEEE 1386.1 (PMC), and provides a subset of the PICMG 2.15 PTMC Configuration 2 features. The Pm8540 operates at 0° to 55°C from a 3.3 or 5 VDC power supply, consumes 11.5W typical and is RoHS/WEEE compliant. Software support includes Carrier Grade Linux. Price in OEM quantities is \$759.

Artesyn Communication Products  
Madison, WI.  
(608) 831-5500.  
[www.artesyncp.com].

### Dual PowerPC Card Features Programmable Processor Speed

Since no two defense applications are exactly alike, each has its own unique requirements for power consumption and operating speed. What if it were possible to change the processor's speed to lower power consumption, and then reprogram it when requirements change? Military designers can do exactly that with the single/dual MPC7447/A PowerPC PrPMC from Curtiss-Wright Controls Embedded Computing. The processor core frequency is software-programmable to operate between 500 MHz and 1 GHz. Once application software has been developed, the PMC-106's power consumption can be reduced to the minimum possible for a given application by reducing the operating frequency.

The VITA-32-compliant PMC-106 PrPMC provides up to 256 Mbytes of ECC-protected DDR-250 SDRAM and 64 Mbytes of flash. The card's PCI-X interface supports 64-bit/133 MHz transfers. It is backward compatible



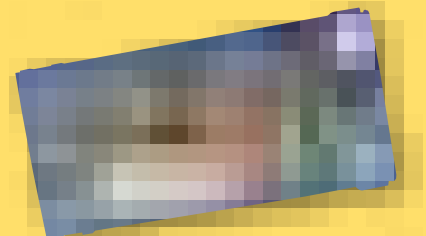
with 32-bit or 64-bit host carrier cards from 33 to 133 MHz. The module can act as the host (monarch) of the local PCI bus or as a peripheral (non-monarch) on the local PCI bus.

A single 10/100/1000Base-T Ethernet port as well as two EIA-232/422 asynchronous serial ports are available through the Pn4 connector to the rear panel. Two thermal sensors, 8 Kbytes of FeRAM, JTAG emulation ports and six discrete LVTTTL signals round out the peripherals. The PMC-106 does not support front panel I/O, but uses the Pn4 connector to route out all rear panel I/O. The card's Discovery II bridge chip provides a four-channel DMA controller, typically used for managing transfers between processor node memory banks and transfers to and from PCI devices. Price starts at \$4,000.

Curtiss-Wright Controls Embedded Computing  
Leesburg, VA.  
(703) 779-7800.  
[www.cwcmbedded.com].

### Dual 7448 PrPMC Module Boosts Multiprocessing

When PrPMCs first emerged several years ago, most were pretty simple, containing only a processor, main memory and a PCI interface. Back then, no one expected them to offer the same leading-edge computing performance as their larger 6U cousins. But today's crop of



PrPMCs integrate some of the fastest CPUs available. An example is Extreme Engineering Solutions' XPedite6200, a symmetric multiprocessing (SMP) platform that is the first dual-processor MPC7448 PrPMC. Several ATCA carrier cards can host up to four XPedite6200s, providing eight total PowerPCs in a single ATCA slot.

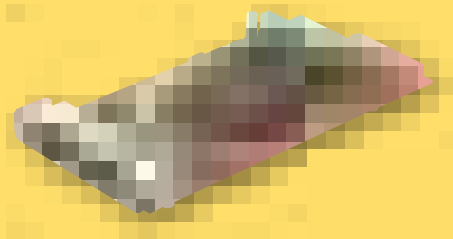
The XPedite6200 features dual Freescale 7448 PowerPCs operating at up to 1.4 GHz and the Marvell MV64460 Discovery III chipset, with a frontside bus speed of up to 133 MHz. AltiVec support lets users take advantage of the processor's real-time vector processing capabilities. Memory provided is up to 1 Gbyte of DDR SDRAM operating at up to 266 MHz and up to 128 Mbytes of flash.

A 64-bit, 133 MHz PCI-X bus interface is provided. Possible RS-232 serial configurations and possible Ethernet configurations each include one front panel port and one P14 port, or two P14 ports. PTMC P14 I/O supports PTMC Configuration 5 Ethernet. A front panel Bellcore 1089-compliant Ethernet port is available for development or craft port usage in the field. Operating temperature is 0° to 70°C from a 3.3, 5 or 12V power supply. A Linux Support Package (LSP), VxWorks Board Support Package (BSP) and QNX BSP are available. XPedite6200 is available immediately with QNX or Linux SMP software. Single quantity pricing starts at \$3,495, with OEM volume pricing below \$2,000 depending on volume, memory and processor configuration.

Extreme Engineering Solutions  
Madison, WI.  
(608) 833-1155.  
[www.xes-inc.com].

### PrPMC Card Integrates 440GX PowerPC With PCI-X

In applications where I/O throughput and low power are equally top priorities, it's hard to beat a PrPMC architecture that can accommodate both. One example is GE Fanuc's PMC721TX, a PrPMC that integrates the low-power IBM PowerPC 440GX processor with up to 512 Mbytes of 133 MHz ECC DDR SDRAM, 8 Mbytes of onboard flash and a 133 MHz PCI-X bus interface. Operating at up to 800 MHz, the PMC721TX features high bandwidth and processing capabilities as well as low power consumption, making it suitable for I/O-intensive communications and networking applications.



The optimized architecture of the PMC721TX offers affordability without compromising high bandwidth and processing performance. The modular approach to the addition of processing capabilities to the PMC721TX gives design engineers an easy way to quickly upgrade existing systems without adding significant cost. Fully compliant with IEEE 1386 and ANSI/VITA 32 for PrPMC, as well as PICMG 2.2, the PMC721TX can be configured to run in monarch mode as the system controller or in non-monarch mode as a dedicated I/O processor.

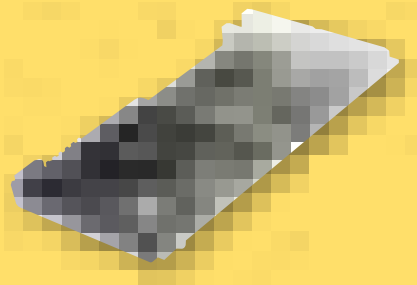
The PMC721TX provides front panel support for two 10/100/1000BaseT Ethernet ports and one RS-232 serial port. Also included is a JTAG interface for board level debug, watchdog timer and real-time clock. Operating temperature is 0° to 60°C from a 3.3 or 5V power supply, and typical power consumption is 12.5 watts. The PMC721TX supports Linux and VxWorks. Pricing starts at \$1,350.

GE Fanuc Embedded Systems  
Huntsville, AL.  
(256) 880-0444.  
[[www.gefanuc.com](http://www.gefanuc.com)].

### PowerPC Board Boasts 333 MHz DDR SDRAM

The Freescale MPC7447A/7448 PowerPC processors are known for both high performance and low power consumption. This combination is a boon to highly integrated defense applications such as network control and signal processing, especially on a PrPMC board. Interface Concept brings the MPC7447A/7448 PowerPC processor onto a PrPMC in its IC-e6-PMCa module.

The processors' PowerPC e600 core delivers a peak performance of 2310 Dhrystone 2.1 MIPS at 1 GHz, while the MPC7448 is expected to exceed 1.5 GHz. The module provides up to 512 Mbytes of 333 MHz ECC DDR SDRAM and 64 Mbytes of flash EPROM. The MPC744A also integrates two 32 Kbyte L1 caches for instruction and data, and a 512 Kbyte L2-ECC cache. The Marvell MV64460 Discovery III chipset adds 2 Mbytes of high-speed SRAM, two XOR DMA and four IDMA engines. An optional backside SO-DIMM site is provided.



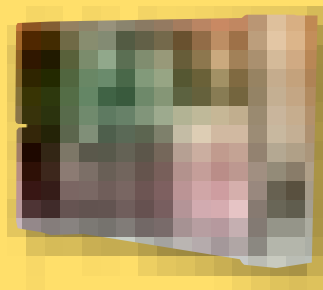
A 64-bit PCI or PCI-X controller allows the IC-e6-PMCa to be used in several PMC or PrPMC configurations in compliance with PCI 2.2 or PCI-X. The board can be configured in monarch or non-monarch mode. Other features include three Gigabit Ethernet ports, two multi-purpose serial controllers, backup SRAM, RTC, a temperature sensor and a JTAG/COP interface for probe debugging. The IC-e6-PMCa currently supports VxWorks and Linux. Pricing starts at \$2,000.

Interface Concept  
Briec de l'Odet, France.  
+33 (0)2 98 57 30 30.  
[[www.interfaceconcept.com](http://www.interfaceconcept.com)].

### Pentium M Card Sports 400 MHz System Bus

Processor PMCs have spurred on an interesting design phenomenon among vendors that make both PrPMCs and larger SBCs. Because PrPMCs by definition comprise the central computing elements of an SBC, board designers can easily recast that design into other form-factors such as CompactPCI.

Exemplifying that trend is a PrPMC board from Mercury Computer Systems that is also available in a 6U CompactPCI form-factor.



Based on the Pentium M 1.1 GHz Pentium M processor with 1 Mbyte on-die L2 cache, the PrPMC Cheetah PCR-150 operates at 1.1 GHz core frequency. The board incorporates up to 1 Gbyte of single-channel 64-bit DDR 333 SDRAM with ECC, and the Intel 855GME memory controller that supports a 400 MHz system processor bus.

An Intel 82546EB provides PICMG 2.15 PTMC-compliant dual Gigabit Ethernet links on the PMC Pn4 connector through a 64-bit, 66 MHz PCI-X bus on the Intel 6300ESB I/O controller hub. A PLX PCI6540 PCI-X-to-PCI-X bridge provides 64-bit 133/100/66 MHz PCI-X or 66/33 MHz PCI bus operation on the PMC interface. Other interfaces include a front panel VGA HD15 interface, a CompactFlash socket, a 1 Mbyte firmware hub and, on the PMC Pn4 connector, a Serial ATA 150 interface, four USB 2.0 ports and two serial ports. The board supports operating temperatures of 0° to 55°C. Price is \$2,475.

Mercury Computer Systems  
Chelmsford, MA.  
(978) 256-0052.  
[[www.mc.com](http://www.mc.com)].



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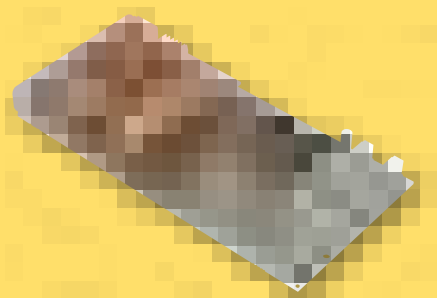
with companies mentioned in this article.

[www.cotsjournalonline.com/getconnected](http://www.cotsjournalonline.com/getconnected)

## PrPMC Weds 1.3 GHz PowerPCs with 2 Gbytes SDRAM

As the originator of the Processor PMC standard, Motorola Computer Group has maintained a steady stream of PrPMC products over the years. Instead of treating PrPMC as a trailing-edge standard, its strategy has been to share the basic core computing design between corresponding PrPMC and VME SBCs.

Motorola's latest PrPMC offering is the PrPMC-280, an SMP platform featuring a single/dual MPC7447 PowerPC processor built with AltiVec technology that enables speeds of up to 1.3 GHz, along with up to 512 Kbytes of integrated L2 cache. The card provides dual 1 Gbit Ethernet connectivity and up to 2 Gbytes of DDR SDRAM. Also on board is a Marvell MV64360 Discovery II system controller with



up to 2 Mbytes of integrated SRAM, up to 128 Mbytes of flash and 64-bit/66MHz PCI and dual serial interfaces. Ethernet can be routed to the front panel or to the Pn4 connector for carrier board I/O, and the board can run in monarch or non-monarch mode.

The PrPMC-280 is VITA 32-compatible. It supports Linux SMP software, and loosely coupled multiprocessing for VxWorks. List price starts at \$1,495.

Motorola Embedded Communications  
Computer Group  
Tempe, AZ.  
(602) 438-3000.  
[[www.motorola.com](http://www.motorola.com)].

## 450 MHz PowerQUICC II Card Offers Five Ruggedization Levels

When developing defense applications, it can be really handy to the military system designer to have a choice of ruggedization options. With this in mind, Radstone offers its PrPMCQ2 in five ruggedization levels, from a convection-cooled operating temperature range of 0° to 55°C at one end of the spectrum to a conduction-cooled range of -40° to +85°C at the other end.



The PrPMCQ2, built around the 450 MHz Freescale MPC8280 PowerQUICC II processor, features a communications processor at up to 300 MHz and memory interfaces at 100 MHz. It provides 32 Mbytes of SDRAM and 16 Mbytes of flash, is 64-bit/66 MHz PCI 2.1-compatible, and provides four general-purpose I/O lines. The PrPMCQ2 also offers four high-speed serial channels, capable of RS-232/RS-422/RS-485 operation (software selectable), and configurable for synchronous or asynchronous operation. Two additional channels provide an additional asynchronous capability useful for development debug and deployed operation on lower-speed

traffic lines. A single 10/100BaseT Ethernet channel completes the array of communications options.

The PrPMCQ2 can function in either monarch or non-monarch modes. Its power consumption is extremely low, only 5W typical. BSPs and Enhanced Support Packages (ESPs) are available for VxWorks and LynxOS. Pricing starts at \$2,000.

Radstone Technology  
Woodcliff Lake, NJ.  
(201) 391-2700.  
[[www.radstone.com](http://www.radstone.com)].

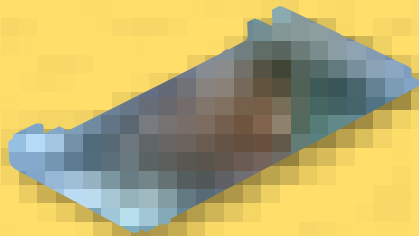




### Pentium M LV/Celeron M ULV Board Delivers Low Power Options

I/O management and packet processing subsystems in applications such as flight computers, software defined radio, and command, control and communications systems require high performance as well as power management schemes. Along those lines, SBS Technologies' PSL09 PrPMC is powered by the 1.4 GHz Intel Pentium M LV and incorporates sophisticated power management technology, eliminating the need for an onboard fan. For very low-power applications, the PSL09 is also available with an Intel Celeron M ULV.

The board includes the Intel 855GME chipset and supports a 33/66 MHz PCI bus. It includes a 400 MHz system bus, a VGA interface and up to 256 Mbytes of 333 MHz DDR SDRAM with optional ECC. The optionally integrated flash with EIDE interface supports up to 256 Mbytes



of flash. Extensive connectivity is provided with four USB 2.0 ports, two Serial ATA channels and two Fast Ethernet ports. Monarch and non-monarch modes are supported.

As an option, the PSL09 features PICMG 2.15 compatibility with the addition of one or two Fast Ethernet links through the Pn4/Jn4 connector. Available in a standard operating temperature range of 0° to 50°C, the board is also available in an extended temperature version operating from -40° to +55°C for more demanding application environments. The PSL09 supports Linux, VxWorks and Windows XP. Pricing in single quantities starts at \$2,140.

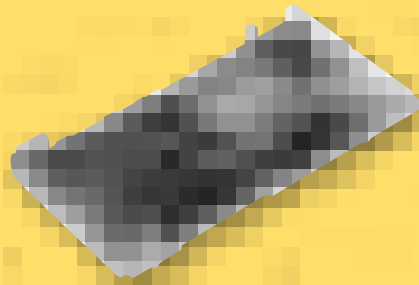
SBS Technologies  
Albuquerque, NM.  
(505) 875-0600.  
[[www.sbs.com](http://www.sbs.com)].

### PrPMC Board Consumes Only 6 Watts

For small, ultra-low-power applications, shaving down the amount of power consumption in a subsystem can be tough. That's why Technobox designed its 3797 PrPMC card to consume only 6 watts typical. The 3797 PrPMC card, based on the 300 MHz Advanced Micro Devices SC2200 GEODE processor, runs off a 3.3V power supply, with 5V for keyboard, mouse and USB ports.

The GEODE processor integrates video, DRAM controller, PCI bus interface, IDE interface, USB and other standard PC peripherals. It provides a 16-bit wide IDE interface available to an onboard CompactFlash device, such as a Hitachi Microdrive. To support rear I/O attachment of IDE devices, the IDE interface also is presented at the PN4 connector. Only the primary IDE interface channel is supported, for either two external drives (master/slave) or one external slave and the onboard CompactFlash master device.

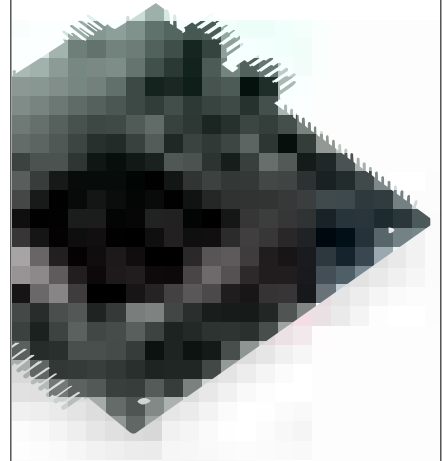
The board supports 128 Mbytes of 100 MHz 64-bit SDRAM. It can be configured in either monarch or non-monarch modes. A PC37364 Super I/O chip provides standard keyboard and mouse ports, as well as a floppy disk controller



interface. The FDC interface is available out the PN4 connector, while the keyboard and mouse are routed to the front panel connector. An onboard Intel 82559 Ethernet controller provides 10/100-TX connectivity via a front-panel RJ45 jack. The 3797 lists for \$995. Quantity discounts are available.

Technobox  
Mount Laurel, NJ.  
(609) 267-8988.  
[[www.technobox.com](http://www.technobox.com)].

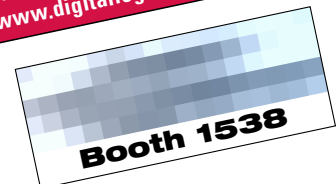
## Low-cost, fanless PC/104 CPU board with 500MHz



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Further information:  
[www.digitallogic.com/msm800sev\\_en](http://www.digitallogic.com/msm800sev_en)



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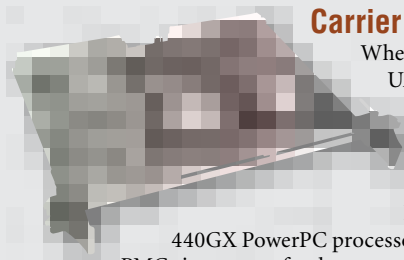
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### Carrier Card Delivers 10X Boost in Image Processing Speed

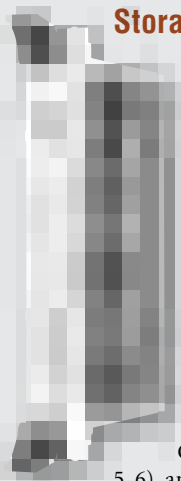
When designing complex, high-performance image processing subsystems used in applications such as UAVs, military engineers want to increase performance and reduce system size. With that in mind, TEK Microsystems has introduced a carrier card that reduces UAV system board count by up to 40%, as well as slashing weight, power and volume.

The PowerRACE-3A combines high-density PowerPC and FPGA processing engines, an onboard switched fabric and PMC interfaces. High-speed I/O and image processing are done in a single slot, while FFT, pulse compression and image processing are handled on PMC carriers. The card uses two 800 MHz

440GX PowerPC processors to support high throughput without incurring host processor overhead. An onboard fabric allows each PMC site to transfer data concurrently to off-board RACE++ ports, FPGA processing or memory, eliminating fabric contention and maximizing overall system performance.

Included with the PowerRACE-3A is the tekX software environment, which provides tools for fabric configuration, buffer management, data transfer, interprocessor communications, data storage/playback and integration of streaming FPGA and I/O modules. The PowerRACE-3A is available 10 to 12 weeks ARO. Pricing begins at \$17,995.

TEK Microsystems, Chelmsford, MA. (978) 244-9200. [[www.tekmicro.com](http://www.tekmicro.com)].



### Storage Blades Provide High Density

High-availability, high-performance military systems are demanding ever more storage capacity, especially as service providers continue to offer more value-add services. With this in mind, Performance Technologies has introduced two 6U storage blades that each offer 1 Terabyte of storage for embedded database, data caching and file serving applications.

The CPC5900 Storage Blade and CPC5910 Storage Expansion Blade are CompactPCI 2.16- and 2.9-compliant. The 6U CPC5900 is a high-density, high-availability NAS or SAN storage blade with two board-level and drive-level hot-swappable SATA hard drives. The onboard, 800 MHz PowerPC processor operates on Performance Technologies' NexusWare Linux development environment. The

CPC5900 supports full RAID arrays (0, 1, 0+1, 4,

5, 6), and can be used as a PXE boot server for automated

deployment of raw boards. Dual Gigabit Ethernet ports provide network connectivity, and 16 Mbytes of flash memory provide expansion space.

The CPC5910 features two board-level and drive-level hot-swappable, enterprise-class SATA hard drives with a SATA interface. When paired with the CPC5900, the CPC5910 supports both NAS and SAN applications. The CPC5900 is priced at \$2,600 in volume, and the CPC5910 at \$1,350.

Performance Technologies, Rochester, NY. (585) 256-0200.

[[www.pt.com](http://www.pt.com)].



### IPv6 VMEbus Managed GbE Switch Platform Targets Mil Apps

A key requirement for network-centric warfare is the support of IPv6. A family of 6U VMEbus Gigabit Ethernet switches from GE Fanuc provides integrated, fully managed Layer 2/3 switching and also supports IPv6.

The new RM921 family is available with 12 (single slot) or 24 (dual slot) front-panel GbE ports, copper and/or fiber connectivity options, conformal coating and an optional 10 GbE uplink port. Based on the Motorola XPC8240 processor and the multilayered Broadcom BCM56302 switch fabric chip, the RM921 is IPv6-compliant with full support for routing and tunneling, and also supports Layer 4-7 functionality. The switches are compatible with current IPv4 deployments and can be fully managed via SNMP, Telnet or a Web server interface.

Advanced QoS functionality includes per-port priority queuing, traffic prioritization and dynamic multicast filtering (IEEE 802.1p), and packet filtering. IPv6 features include IPv6 addressing and specification (RFC 2460), neighbor discovery for IPv6 (RFC 2461), stateless address auto configuration (RFC 2462), ICMPv6 (RFC 2463) and IPv6 over Ethernet (RFC 2464). Pricing starts at \$4,000.

GE Fanuc Embedded Systems, Huntsville, AL. (800) 322-3616. [[www.gefanuc.com](http://www.gefanuc.com)].

### Software Radio Transceiver Boosts Channel Density 16x

Multi-channel, military communications systems such as military radios require high channel density within tight size, weight, cost and power constraints. A new PMC/XMC software transceiver module from Pentek boosts channel density by a minimum of 16x.

The 7140-430 dual transceiver and digital up/downconverter combines a high-density, narrowband, digital downconverter (DDC) FPGA IP core with Pentek's 7140 software radio transceiver PMC module. The 7140-430 provides 256 individually tunable receive channels, compared

to the more typical four to 16 narrowband channels. It includes two A/D and two D/A converters capable of bandwidths to 40 MHz and above for connection to HF or IF ports of a communications or radar system. The 7140 receiver section features two AD6645 105 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter.

In the 7140 module's transmit section, a digital upconverter translates real or complex baseband signals to any IF center

frequency from DC to 160 MHz. Two 16-bit D/A converters then produce real or quadrature (I+Q) IF output signals routed through the module's PCI interface. The module is currently supported with Linux drivers.

Pricing for the 7140-430 starts at \$14,995 with delivery 8-10 weeks ARO.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [[www.pentek.com](http://www.pentek.com)].



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### VX5 Extender Board Provides Easy Access

To provide full access for testing or debugging to a circuit card under test, extender boards must bring the card completely out of its card cage or enclosure. Until recently, VX5 extender boards were not available because of the lack of a right angle receptacle for VX5. Elma Bustronic has developed its VX5 Extender Board for hub slots by engineering a rigid-flex-rigid PCB.

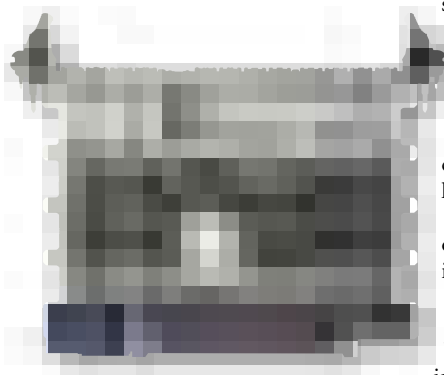
The Elma VX5 Extender Board for hub slots utilizes a right-angle pin connector that plugs into the backplane, connected to a flex circuit wired to the straight receptacle to receive the plug-in board. There are test points for all of the differential pairs on the multi-Gigabit fabric connector for the hub slots. The VX5 Extender boards come in a 10-layer stripline design for the rigid PCB and a microstrip design for the flex circuit portion. Also featured is an ammeter, which measures the current and has a digital indicator on the front panel showing the status.

Lead time is 2-4 weeks ARO. Pricing is under \$3,000, and depends on configuration and volume.

Elma Bustronic, Fremont, CA. (510) 490-7388. [[www.elmabustronic.com](http://www.elmabustronic.com)].

### Zero Latency Circuit Switch for VX5

Military engineers building signal processing systems such as radar, sonar, SIGINT, electronic intelligence and real-time imaging sometimes may require only a few VX5 boards interconnected with point-to-point connections in a custom VX5 backplane using a simple protocol. However, this solution still demands the time and expense needed to develop a custom backplane.

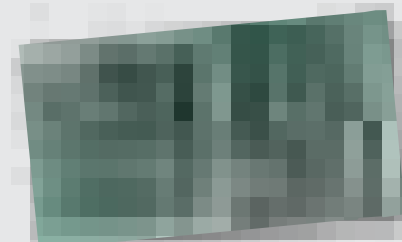


The Phoenix CSW1 circuit switch from VMetro solves these problems by providing the ability to use off-the-shelf VX5 backplanes and change the CSW1's routing topology. VX5 payload cards can be connected together with fast, protocol-agnostic data links. These links can be arranged in any topology.

The Phoenix CSW1 supports 56 1x VX5 backplane data links, each operating at up to 3.2 GHz, enabling intrasystem communications and remote sensor interfaces. Backplane data links can be utilized as 4x payload slot links in off-the-shelf VX5 star backplanes. Additional optional I/O capabilities include up to 12 front-panel transceiver channels

and a short XMC site. The Phoenix CSW1 is available 8 to 12 weeks ARO. Pricing begins at \$7,995. Discounts may apply to customers using other Phoenix products.

VMetro, Houston, TX. (281) 584-0728. [[www.vmetro.com](http://www.vmetro.com)].



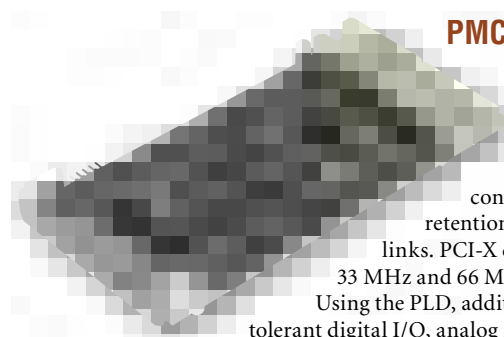
### Conduction-Cooled Audio Card Sports Front and Rear I/O

A conduction-cooled PMC audio card features a single PMC slot with front and rear I/O, widening the options for audio connections in high-performance systems. The ccPMC481 from AcQ InduCom is based on the CrystalClear PCI audio interface controller and the CrystalClear CS4299A SoundFusion audio codec '97.

The ccPMC481 includes four audio connections via the front panel using 3.5 mm stereo connectors. Audio connections can be made via the rear I/O using the optional PIM481-J PMC I/O module, which mounts on a rear transition module and has four 3.5 mm stereo connectors. The audio interface consists of a line input, a microphone input, a line output and a speaker output with an onboard stereo amplifier.

The card also includes a 33 MHz/32-bit PCI interface, supports 3.3V and 5V signaling and has a 5V and 12V power supply. Price is \$640 each.

AcQ InduCom, The Netherlands.  
 +31 (0)412 641922. [[www.acq.nl](http://www.acq.nl)].



### PMC SATA Controller Manages Four Attached Devices

Although not yet mainstream in the high-performance embedded space, Serial ATA is gradually displacing some older drive technologies in high-demand defense applications. A SATA controller from Technobox manages four attached devices.

The Versatile SATA Controller, P/N 4382, provides four 1.5 Gbit/s links on a PMC front panel. Additional features, supported by a PLD, are provided for rear I/O. The PCB mounted connector is a "latching style" version permitting use with SATA cables that have a built-in, positive-retention latch. The board employs an Intel 31244 controller, which connects the PCI-X bus to four SATA links. PCI-X can operate up to 133 MHz under ideal conditions, but the board will also operate in lower speed 33 MHz and 66 MHz buses and in 32-bit and 64-bit modes.

Using the PLD, additional functions can be enabled, including an interface to an I<sup>2</sup>C controller, four UARTs, 5V-tolerant digital I/O, analog inputs and system monitor. A boot EEPROM automatically loads the PLD on power-up. A front I/O-only variant of the controller, P/N 4383, does not incorporate the PLD. The fully populated 4382 lists for \$495. A depopulated variant, the 4383, lists for \$295. Quantity discounts are available.

Technobox, Mount Laurel, NJ. (609) 267-8988. [[www.technobox.com](http://www.technobox.com)].

## RGB/Video/DVI Controller Optimized for Multimedia Apps

An increasing number and variety of military systems must display data accurately on LCD displays. A new controller board from Apollo Display Technologies enables TFT LCDs to be connected to standard graphics/video interfaces.

The PRISMA II controller board, a next-generation version of the company's PRISMA RGB/Video Converter Board, is optimized for multimedia applications. Input signals such as analog RGB, analog video or DVI are converted into TFT-compliant TTL or LVDS signals. Onboard component video support is provided, as well as user-selectable data/power connectivity options and user-defined configuration of each input interface. The board supports resolutions to WUXGA (1920 x 1200) and includes picture-in-picture (PIP) and picture-by-picture (PBP), advanced HMI capability and advanced scaling features such as pan and zoom.

PRISMA II features include component video input, improved video quality and better de-interlacing and improved auto-adjust functionality. The board is compliant with the European Union Restriction of Hazardous Substances (RoHS) directive. An optional power supply up to 24 volts is available. Pricing for the PRISMA II is under \$120 in production quantities of 10K units.

Apollo Display Technologies, Ronkonkoma, NY. (631) 580-4360. [www.apolلودisplays.com].

## Advanced Integrated Recorder Features Windows Screen Recording

Formation's Advanced Integrated Recorders (AIRs) are used widely in air traffic control (ATC) and air defense/C4I systems for after-action review, debriefing, incident investigation and legal recording. Newer ATC and C4I training and simulation systems employ the Windows operating system, but the AIR system previously offered X-Windows screen

recording. A new version now enables Windows screen recording.

The AIR's added functionality enables all activities that occur on the screens of PCs and workstations

employing the Windows 2000 or Windows XP operating systems to be recorded. All mouse movements, menu selections, text entries and window views can be capture and time-tagged. Recordings can be replayed synchronously with voice communications, radar data, LAN data and video, to provide accurate re-creations in complex ATC, C4I or training scenarios.

The AIR system is scaleable and expandable. Configurations range from a stand-alone 1U server with as few as four voice channels to a networked storage system that supports over 1,000 screen, data and voice channels. Pricing starts at \$10,000, depending on configuration.

Formation, Moorestown, NJ. (856) 234-5020. [www.formation.com].

## VMEbus SBC Sports Dual PPCs

Demanding military workstation applications, like systems used for training, simulation and targeting, need lots of processing power. A new VMEbus-based SBC from General Microsystems delivers a big performance increase over past generations of SBCs with dual 7447 PowerPCs.

The Maverick SBC's dual 7447 PPCs operate at 1 GHz with 512 Kbytes of on-die L2 cache. The board supports symmetric multi-processing (SMP) and 128-bit AltiVec technology, and incorporates the Discovery III system controller. It has full PC functionality, including dual USB and Ultra SCSI 320/160, and two 64-bit 66/100 MHz PMC expansion sites, one with rear I/O.

The board includes up to 1 Gbyte of DDR SDRAM SODIMMs, 32 Mbytes of application flash and 2 Mbytes of bootable flash. For flexibility in setup and operation, the V394 offers three Gigabit Ethernet ports, one multi-protocol sync/async serial port, a parallel port, 21 discreet digital I/O lines and front-panel LEDs.

Support for Linux, QNX and VxWorks is standard. Pricing starts at \$2,600 each in quantities of 100 units.

General Microsystems, Rancho Cucamonga, CA. (800) 307-4863. [www.gms4sbc.com].

## Rugged ETX Module Boasts Notebook-Style Power Management

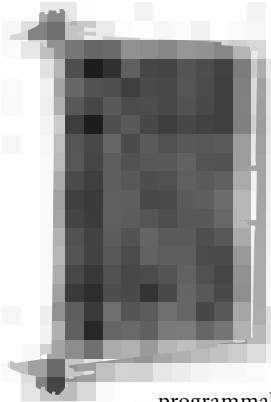
Ruggedized, battery-powered embedded computers have appeared for several military uses. But these can be bulky and without enough power management options. A rugged ETX module with full notebook-style ACPI 2.0 power management will help military engineers design handheld and vehicle-mounted embedded computers with long battery life, vibration resistance and long production life.

The ETX 802 Computer-on-Module (COM) features performance of up to 1.4 GHz with operation to 85°C. ACPI S3 suspend-to-RAM technology provides extended battery life and very fast wake-up from a low-power state. The module includes the Intel 855GME chipset, up to 1 Gbyte of ECC or non-ECC DDR RAM, four USB 2.0 ports, dual EIDE interfaces, 10/100 Ethernet, PCI expansion and compliance with the European Union Restriction of Hazardous Substances (RoHS) directive.

AMI BIOS provides full support for wake-up devices. ETX 802 includes legacy support with ISA bus expansion, two serial ports, PS/2 keyboard and mouse, parallel port and floppy-over-parallel support. QuickStart Kits include drivers and Board

Support Packages (BSPs) for Windows XP, Windows XP Embedded, Windows CE 5.0, VxWorks, QNX and a full Linux 2.6 distribution (Fedora Core 3). Prices start at under \$600 in moderate quantities.

Ampro Computers, San Jose, CA. (408) 360-0200. [www.ampro.com].



### VME Comms Card Offers Multiple I/O Functions

Gone are the days when it was necessary to have a separate VME board for every type of I/O interface. Now several can be crammed onto a single-slot card. Along just such lines, North Atlantic Industries (NAI) has announced the availability of a multi-function, single-slot, VME Communications Card. This card eliminates the complexity and size constraints of using multiple, independent, single-function communication cards. The 64D1 VME card accommodates three independent function modules, each of which can include: 2 channels of Dual Redundant MIL-STD-1553 BC/RT/MT, 6 channels of Synchronous or Asynchronous RS-232C/RS-422/RS-485, 8 channels of Profibus, 48 channels of Discrete I/O or 48 channels of TTL I/O.

For increased flexibility, each of the functions of the 64D1 is highly programmable at the channel level. Continuous background (BIT) testing is performed on all functions and channels. This testing is totally transparent to the user, requires no programming and doesn't interfere with the normal operation of the card. The 64D1 is available with operating temperature ranges of -40° to +85°C and 0° to +70°C. Conduction-cooled versions with wedgelocks are also available. Pricing starts at \$2,500 each, for 100 piece quantities.

North Atlantic Industries, Bohemia, NY. (631) 567-1100. [[www.naii.com](http://www.naii.com)].

### Pentium-Based Multi-SBC System Has MPI Link

When you need to develop complex multiprocessing applications, it's helpful to start with a ready-to-use solution and not have to fuss with the integration multiple SBCs. With that in mind, IBM and Thales introduced the PowerMP6, a turnkey computer system designed to allow for maximum software productivity. The PowerMP6 consists of multiple Pentium-M boards in a 19-inch rack. Running Red Hat Linux on the Intel processors supports software productivity and portability through an extensive set of open source and commercial tools and libraries. Performance is dictated by the number of Pentium M processors the system runs and the PowerMP6 available in various customized configurations of up to eight processor boards in a rack. With the integration of the brand new PENTXM2 dual core SBC, the PowerMP6 system will migrate to dual core Pentium M technology by the end of this year.

The PowerMP6 features an optimized message passing interface (MPI) for multiprocessor communications and contains software tools geared for such tasks as real-time performance analysis, remote control operations and monitoring system management. Activities such as system reset, reboot and access to system administration and configuration control can be undertaken from any external computer equipped with a Web browser. Pricing starts at \$31,000.

Thales Computers, Toulon, France. (33) 4 98 16 34 00. [[www.thalescomputers.com](http://www.thalescomputers.com)].

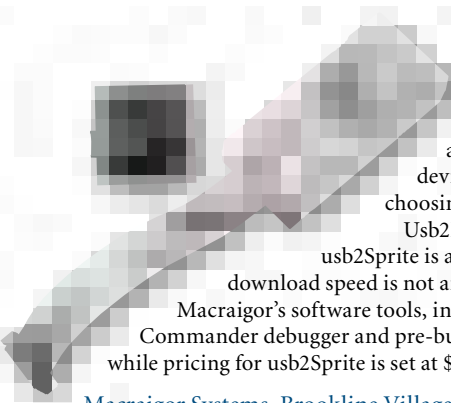


### Hi-Rel DC/DC Converter Family Powers Up to 120W

It's no small task for a DC/DC converter to function continuously in rugged environments typically encountered in military and aerospace applications. Protection features and low internal component count are both critical. International Rectifier follows such a path with their new high-reliability (Hi-Rel) AHP line of high-power, high-density hybrid DC/DC converters for digital and analog circuits that require a well-regulated power source. The AHP series offers as high as 87 percent efficiency and a power density of as much as 84W per cubic inch.

The AHP input over-voltage protection will shut down the converter at 110 percent of the maximum-rated input voltage and will re-start when the input voltage drops below this threshold. The AHP converters also feature high power density with no de-rating over the temperature range of -55° to +125°C. This series is offered as part of a complete family of converters providing single and dual output voltages and operating from nominal 270 VDC input and outputs of 3.3, 5, 6, 8, 9, 12, 15, 28, ±5, ±12 and ±15V and power ratings from 80 to 120W. Pricing is in the high \$700 range each device in quantities of 100.

International Rectifier, El Segundo, CA.  
(800) 865-8247. [[www.irf.com](http://www.irf.com)].



### USB 2.0 Interface Devices Do JTAG Debug

Like most I/O technologies that were born in the PC world, USB has found its way into the embedded systems realm. Making good use of USB 2.0, Macraigor Systems announced the usb2Demon and usb2Sprite, two new USB 2.0 JTAG debug interface devices. These new devices are immediately available for ARM, Xscale and PowerPC processors. The usb2Demon and usb2Sprite devices are identical in functionality, but differ in speed to provide embedded developers with flexibility in choosing an appropriate price/performance ratio for their projects.

usb2Demon provides a significant download speed improvement over earlier JTAG tools, while the usb2Sprite is a low-cost, slower version of the device for price-sensitive projects or situations where maximum download speed is not an issue. Both new devices support Windows and Linux hosts and are fully compatible with all of Macraigor's software tools, including the Flash Programmer, J-Scan suite of JTAG hardware debug tools and the free, low-level OCD Commander debugger and pre-built GNU tools suite. Both USB 2.0 devices are immediately available. Pricing for usb2Demon is \$750, while pricing for usb2Sprite is set at \$210.

Macraigor Systems, Brookline Village, MA. (617) 739-8693. [[www.macraigor.com](http://www.macraigor.com)].



## Rugged Cases Meet Rigorous NATO/European Standards

On the battlefield, rugged cases are a critical tool for keeping electronic equipment protected. Pelican Products has announced that its line of high-impact, watertight Protector Cases has been certified with the NATO (North Atlantic Treaty Organization) Stanag 4280 and Def-Stan 81-41 quality testing standards. The Stanag 4280 and Def-Stan 81-41 standards for military use are embraced by the NATO countries as the European equivalents to the Mil-Spec certification in the United States. Both sets of criteria subject the cases to an extensive battery of standardized endurance and quality tests designed to simulate extreme situations. Pelican Protector Cases withstood high and low temperatures for extended periods of time—up to 131°F for 48 hours and as low as -4°F for 16 hours.

Pelican Protector Cases offer a fully stackable design, boasting nearly 14,000 cubic inches of possible storage space in the line's largest cases. To ensure easy and immediate access, most cases feature double-throw latches that have been tested to a failure threshold of nearly 400 pounds, but open with a light pull. Stainless steel reinforced padlock protector holes (on most models) are also featured for added security.

Pelican Products, Torrance, CA. (310) 326-4700. [[www.pelican.com/military](http://www.pelican.com/military)].

## PICMG 1.3-Style Opteron Board Supports PCIe and PCI-X

The AMD Opteron processor is standing forth as an early favorite among emerging dual-core microprocessors. WIN Enterprises uses it on its MB-06048, a PICMG 1.3-style SBC

that can be powered by one or two single- or dual-core AMD Opteron processors. The new SBC features PCI Express and PCI-X 64-bit/133 MHz support, plus onboard video and 3-port LAN capability. A stackable HyperTransport technology-based extension card can support a second CPU to provide the dual, dual-core CPU configuration—four processing cores—for support of processing-intensive applications.

In a small board size—13.330 in. x 4.976 in. form-factor—the board offers ATI 64MB M9 graphics, three 10/100/1000 Gbit Ethernet LAN ports and four USB ports. The board features a 4X Serial ATA with RAID, a 16-lane PCI Express slot and 64-bit/133 MHz PCI-X. Two memory slots with up to 8 Gbytes of DRAM are on board along with a standard IDE interface. A MB-06048 SHB that accommodates one single- or dual-core AMD Opteron processor costs \$1,000. Configured with a CPU extension board adds an additional \$250. These prices are without CPUs and memory.

WIN Enterprises, N. Andover, MA (978) 688-2000.  
[\[www.win-ent.com\]](http://www.win-ent.com).

## Rugged 3U cPCI Card Does Gbit Ethernet Switching

The Everything-over-IP (EOIP) concept is becoming well entrenched for battlefield networking. That's driving a need for compact, lightweight Gbit Ethernet switching in harsh environments. Serving such needs, Curtiss-Wright Controls Embedded Computing has announced the new 3U CompactPCI SCP/DCP-681 Compact SwitchBlade Gbit Ethernet switch/router. This 10-port, fully managed, intelligent multilayer (layer 2/layer 3) card is available in both air-cooled (SCP) and conduction-cooled (DCP) configurations. It provides up to ten wire-speed 10/100/1000 Mbit/s Ethernet interfaces in a single 3U cPCI slot.

The SCP/DPC 681 design provides wirespeed, non-blocking performance on all ten (10) of its 1 GbE ports over the cPCI backplane. With address tables and buffer memory fully integrated on chip, the SCP/DPC 681 can support advanced full-duplex end-to-end flow and congestion control that facilitates reliable operation. To ease and speed system development, Curtiss-Wright also offers an optional 3U cPCI rear transition module that can be used to connect end nodes

using standard RJ45 cables. DCP (conduction-cooled) versions of the card can also be supported with an optional 10-port LEDS front-panel plug-in. Pricing for the SCP/DCP-681 starts at \$9,100.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA.  
 (703) 779-7800. [[www.cwembedded.com](http://www.cwembedded.com)].

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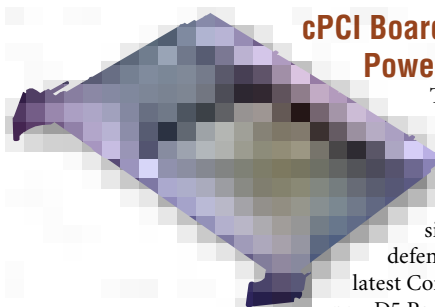
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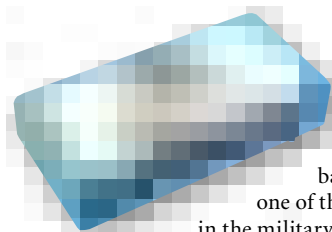
## cPCI Board Blends FPGA and PowerQUICC III

The military didn't warm to CompactPCI overnight. But now that it's mature and established, it has won significant mindshare in the defense market. MEN Micro's latest CompactPCI board is the new D5 PowerPC SBC. Based on the PowerQUICC III family of processors,

the board also includes a Cyclone FPGA from Altera that enables the onboard configuration of application-specific I/O or other functionality.

For added I/O functionality, the D5 features two slots for PMC mezzanine cards that support both front- and rear-panel connectors. The board has one 32/64-bit, 33/66 MHz PCI bridge to the CompactPCI bus. Onboard memory resources include up to 4 Gbytes of ECC DDR SDRAM main memory and 1 Gbyte or more of NAND flash memory for program or data storage. Two Gbit Ethernet and one Fast Ethernet ports are implemented as rear connections. One RS-232 port is located on the front panel for debugging purposes or, as an option, the board can be configured with an interface to Compact Flash. Another serial channel is available on the board and is connected via one of MEN's SA-Adapters. An IDE connector can be used for peripherals, such as an onboard hard disk. Available now, pricing starts at \$2,154 for single units.

MEN Micro, Dallas, TX. (512) 267-8883. [[www.menmicro.com](http://www.menmicro.com)].

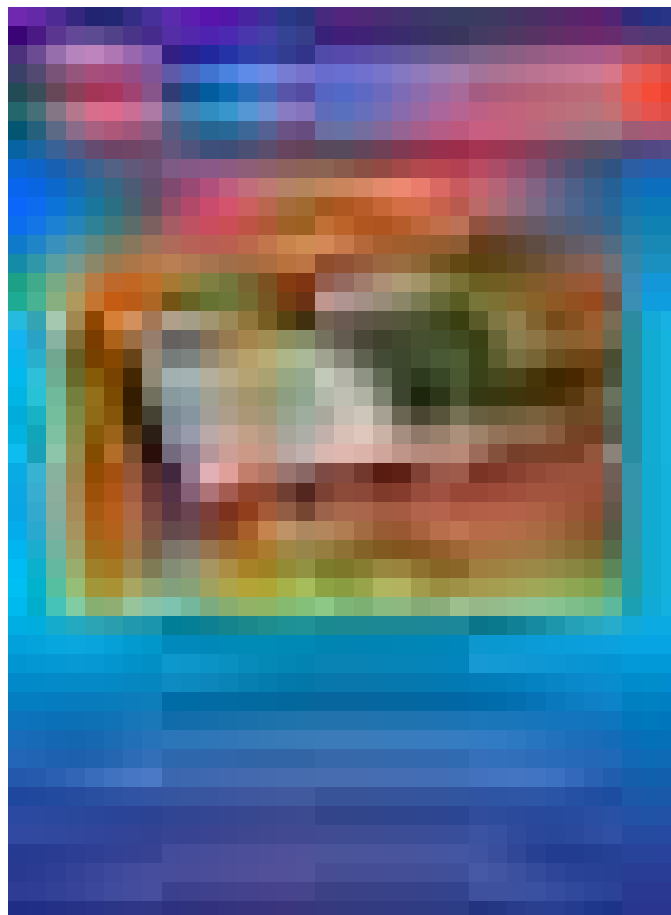


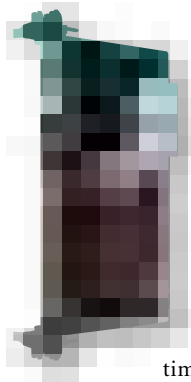
## DC/DC Converters Target Embedded Signal Processing

The area of portable mobile battery-driven equipment represents one of the most dynamic areas of development in the military. High-density DC/DC conversion is critical in that realm. Martek Power addresses that market with the release of the LNB series, a new product family of high-density, ultra low-noise, fully isolated DC/DC converters. The LNB series offers output ripple of 10 mVp-p and operates over input voltage ranges of 4.5 to 7 VDC, 8 to 16 VDC and 18 to 36 VDC, making them ideally suited for embedded signal processing applications. Packaged in an industry standard size of 1.0 x 2.0 x 0.4-in., the low-profile DC/DC LNBs feature a rated power of 10W and precisely regulated single output voltages of 3.3V, 5V, 12V and 24V. Efficiency is over 85 percent.

The LNB series feature six-sided continuous shielding, output overvoltage protection, short circuit protection, synchronization, a wide -30° to +100°C case operating temperature range and 1500 VDC input/output isolation. The MTBF is rated at 1,000,000 hours. In addition, with the majority of power supply vendors discontinuing 5 VDC and 12 VDC input DC/DC converters, the LNB, with its industry standard footprint, provides a perfect drop-in replacement. The LNB series are priced at \$30.00 per unit for volume orders.

Martek Power, Los Angeles, CA. (310) 202-8820. [[www.martekpower.com](http://www.martekpower.com)].



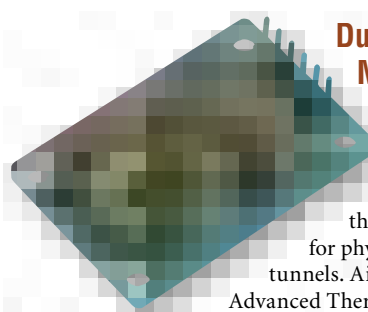


### Time-to-Digital Converter Rides CompactPCI

Military test applications, like explosive testing and time-of-flight measurement in mass spectrometry and 3D mapping, require conversion of time measurements into the digital domain. Supporting that need, Acqiris now offers a wide-range, single- and multi-start time-to-digital converter (TDC) module. The new Acqiris TC840 CompactPCI module, with 50 ps timing resolution, is designed specifically for use in large scale experiments. In addition, the TC840 features inputs with programmable thresholds, making the module ideal for measuring the time of the rising or falling edge of very fast trigger events.

The TC840, a wide-range, single- and multi-start TDC, has thirteen identical hardware channels. Twelve channels are independent stop inputs; the thirteenth is the common start. Time measurement on the TC840 can be based on either the internal low jitter (<3 ps rms), high-stability ( $\pm 2$  ppm) clock source, or an external 10 MHz reference input. Digitized data is fed directly to the onboard FPGA-based data processing unit. This handles the data and subsequent fast readout with direct memory access (DMA) mode, for increased data throughput to the PC. Pricing for the TC840 wide range single- and multi-start time-to-digital converter starts at \$11,990.

Acqiris USA, Monroe, NY. (877) 227-4747. [[www.acqiris.com](http://www.acqiris.com)].



### Dual-Sensor Board Measures Temp and Air Velocity

While a lot of today's aircraft tests can be done using computer simulation, there's still no substitute for physical tools such as wind tunnels. Aimed at just such applications,

Advanced Thermal Solutions has introduced the ISD board, which is designed to measure air temperature and velocity from two independent sensors.

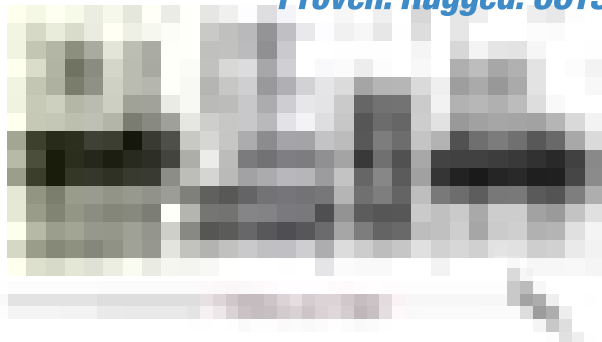
The ISD's sensors provide high-speed data rates via analog voltage outputs that range from 0 to 5 volts per sensor. The board can be used to control various devices or to provide read-out data for display systems. Several ISD boards can be integrated onto one PCB for multi-point measurement of velocity, temperature or both.

The compact ISD temperature and air velocity measurement board has a small 1.60 by 1.06 inches (39.7 by 27.0 mm) platform, and is just 0.41 inches (10 mm) in height. Total weight is 6 grams. The high-precision sensors are calibrated at 0.3 to 50 m/sec air velocity range, for both low (natural convection) and high flow rates. Temperature measurement capability ranges from -30° to 150°C. Velocity measurements range from 0 to 50 m/s (10,000 ft/min). Starting price for the standard ISD board with two sensors is \$657.00.

Advanced Thermal Solutions, Norwood, MA. (781) 769-2800. [[www.qats.com](http://www.qats.com)].

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### DSP Board Provides 72 Gips of Processing Might

Real-time parallel processing is vital to applications ranging from image processing to signal intelligence. Feeding that need, Signatec has introduced the PMP1000, PCI-X board sporting nine 1 GHz TI TMS320C6414T DSPs. Mapped directly into the eight processing DSPs is 64 Mbytes of memory. Operating at a clock rate of 1 GHz, each DSP is capable of executing up to eight instructions per clock cycle for a

peak processing performance of 8 GIPS per DSP, or 72 GIPS for the entire board. An open source connector allows for total customization with any bus, or combination of buses.

Three data interfaces on the PMP1000 allow for communication to the outer world. The primary interface is the PCI-X host interface. The board can also be operated in lower performance PCI slots, including both 64 and 32 bits from 133 MHz to 33 MHz.

The second interface is the Signatec Auxiliary Bus (SAB), which allows for a high-speed connection to other Signatec boards and can sustain transfer rates up to 500 Mbytes/s. The third external bus interface allows for high-speed external interface connections up to 500 Mbytes/s to any customer-specific bus or combination of buses. Pricing for the PMP1000 starts at \$8,400.

Signatec, Corona, CA. (951) 734-3001. [[www.signatec.com](http://www.signatec.com)].



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**Dr. Robert F. Leheny,**

Deputy Director, Defense Advanced Research Projects Agency (DARPA).

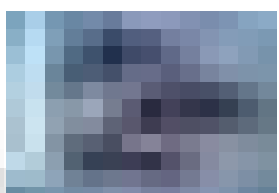
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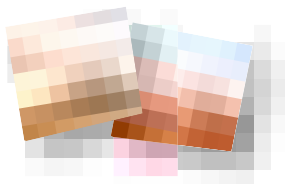
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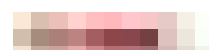
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## Coming Next Month

If you're reading this you're in good company. In fact, there's 38,000 of you out there that receive and read *COTS Journal*. And that number will be increased in April with a bonus circulation at the Second Annual Military Embedded Electronics and Computer Conference (MEECC) in Long Beach, California, May 16-17. Look for special preview material on the conference in the pages of our April issue.

Here's what else we've got cooking for the April issue of *COTS Journal*:

- **PC/104 in the Military.** PC/104 continues to gain fans in the military realm thanks to its compact size and inherent ruggedness. Sweetening the deal, a number of special enclosure techniques are used to suit it for extremely harsh environments. This series of articles looks at those techniques, the levels of ruggedization available and some of the special applications using PC/104 and PC/104-Plus. An update on the new PC/104 follow-ons, EPIC and EPIC Express, will be included also.
- **VME for the Next 25 Years : Part II.** In March *COTS Journal* we presented Part I of our special "VME for the Next 25 Years" feature section. Part I examined how the VME community is providing military system designers an upgrade path by blending switched fabric technologies with VME into the latest VITA specs. This month, in Part II, we'll share what top executives from VME board suppliers in the defense market are saying about the next 25 years of VME. Also included is a timeline illustrating the details where VME's been and where it's going.
- **Safety-Critical Systems & Software.** The military and aerospace industry mandates rigorous technical and process requirements for safety-critical computing. Standards such as DO-178B and ARINC-653 are now an entrenched part of the major embedded OS vendors' offerings. Articles in this section update readers on those standards and how they're being implemented.
- **PXI/VXI Boards and Subsystems.** The PXI bus form-factor, and its older cousin VXI, have become staples as instrumentation and test solutions for complex, high-performance military systems. This Tech Focus section updates readers on the latest trends in these technologies along with a focused, product album of representative boards in these architectures.



# Editorial

Jeff Child, Editor-in-Chief

**O**ne vivid memory from my former life as an engineer is the dry sense of humor of my fellow system designers and test engineers in the engineering department. We used to have a sign that said “If it Works, Fix It”, which always drew laughs from visitors. It had a ring of truth, because—as is part of the engineer’s nature and process—our job centered on making things work and improving designs to make them work better. Engineering is naturally an iterative process—in other words, success is achieved after iterations of prototypes and testing. Certainly sophisticated design tools help reduce the number of iterations required, but “correct from the start” designs are still far from the norm, even in this age of advanced automated design, modeling and simulation technologies.

It’s from that perspective as a former engineer that I appreciate the worthy strides the DoD has been making to come to grips with the problem of defense acquisition reform. Last August in this column I examined the progress of the DoD’s Defense Acquisition Performance Assessment (DAPA) project, Deputy Secretary of Defense Gordon England’s initiative aim to, in his words, move to “a simplified acquisition process that restores confidence in the acquisition system and supports the war on terror as a primary goal.”

Since then, I’ve kept an eye on the progress of that project—up until its completion in January—and have been intrigued with a lot of the issues it’s tackled. I confess it was hard to keep deep skepticism from clouding my view of the project—how many times in the past two decades alone have similar panels studied the acquisition process, without showing much improvement? That said, documents released in DAPA’s public meetings revealed some interesting insights and themes of discussion, many of which had the ring of stuff that our design engineer readers deal with—such as process improvement and hardware/software integration.

DAPA panel member, retired U.S. Army General Paul Kern, remarked that there’s nothing in the policy that stresses continuing process improvement. Kern is the former Commanding General of the Army Materiel Command, and now Executive Advisor and Senior Counselor for The Cohen Group. He remarked on how such major corporations like General Electric focus on a six sigma process, and Toyota, a lean production process. “Everyone who’s looking at things is not satisfied with the status quo,” said Kern, “Yet we seem to continually march right to writing it down in the regulation and policy and calling it good, as opposed to continuously trying to improve it.”

Another panel member, Frank J. Cappuccio, v.p. and gen-

eral manager of Advanced Development Programs at Lockheed Martin Aeronautics, made an interesting point about system integration and how it’s unaccounted for in schedules. He explained that assessing the technology risk for a jet engine is possible and that assessing the technology risk for a piece of software is possible. But, in contrast, there’s no way to assess the time or cost it will take to get that software and that engine working together in a lab. “I’ve actually looked back and tracked the overruns on major programs. The amount of lines of software and the coding of that software isn’t the problem,” he said. “The problem is the integration.”

The end goal of the DAPA project was to issue a report designed to influence the Quadrennial Defense Review. The DAPA report, which went public at the end of

January, included, I think, a wealth of good recommendations for reform. One section that most interested me focused on Technology Maturity. Many of the major, complex programs underway have been widely criticized for their dependence on immature technologies. This section talks about how incorporating high-risk technology in systems generally leads to significant cost and schedule impacts.

The report cites an example where a major defense contractor in their commercial business follows a ten-step process in the development of a new product. Progressing beyond Step 6—which for military programs equates to the DoD’s System Development and Demonstration Phase—cannot occur until requirements are fixed, development and production costs are known, and technology is mature. An advantage of that model is that only modest resources are expended up through Step 6. The DAPA report suggests that this process should be emulated in DoD programs.

The conclusion is that because defense acquisitions are so complex, they do not carry management reserves to accommodate the “unknown unknowns” associated with technical immaturity. Programs in their System Development and Demonstration phases may be driving technology, but usually lack any contingency or “fall back” options to an acceptable capability. The DAPA report suggests developing just such contingency plans, technology assessments and exit opportunities in cases where technologies do not mature as anticipated. That will provide Program Managers with ways to take alternative action or stop efforts altogether, if warranted.

Those and many other innovative changes are suggested by the DAPA Project Report. But as the report says itself in its introduction, DAPA won’t ultimately be judged by how well it identified the problems, or even how well it points to the solutions. Rather, it will be judged by what it actually makes happen. ■■

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